

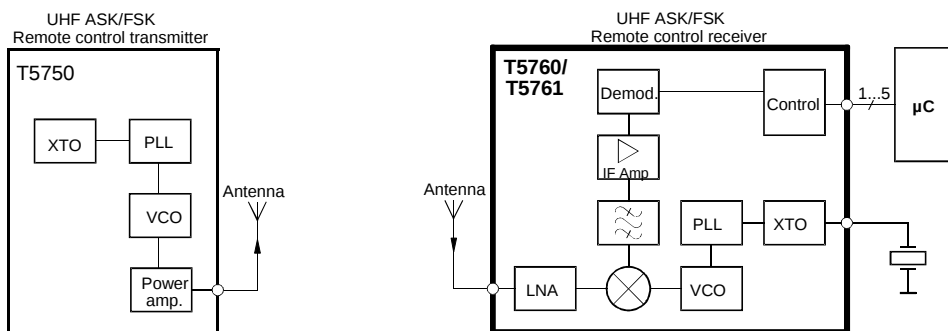
## Features

- Frequency Receiving Range of  $f_0 = 868 \text{ MHz}$  to  $870 \text{ MHz}$  or  $f_0 = 902 \text{ MHz}$  to  $928 \text{ MHz}$
- 30 dB Image Rejection
- Receiving Bandwidth  $B_{IF} = 600 \text{ kHz}$  for Low Cost 90-ppm Crystals
- Fully Integrated LC-VCO and PLL Loop Filter
- Very High Sensitivity with Power Matched LNA
- High System IIP3 (-16 dBm), System 1-dB Compression Point (-25 dBm)
- High Large-signal Capability at GSM Band (Blocking -30 dBm at +20 MHz, IIP3 = -12 dBm at +20 MHz)
- 5 V to 20 V Automotive Compatible Data Interface
- Data Clock Available for Manchester- and Bi-phase-coded Signals
- Programmable Digital Noise Suppression
- Low Power Consumption Due to Configurable Polling
- Temperature Range -40°C to +105°C
- ESD Protection 2 kV HBM, All Pins
- Communication to Microcontroller Possible Via a Single Bi-directional Data Line
- Low-cost Solution Due to High Integration Level with Minimum External Circuitry Requirements

## Description

The T5760/T5761 is a multi-chip PLL receiver device supplied in an SO20 package. It has been especially developed for the demands of RF low-cost data transmission systems with data rates from 1 kBaud to 10 kBaud in Manchester or Bi-phase code. The receiver is well suited to operate with the Atmel's PLL RF transmitter T5750. Its main applications are in the areas of telemetry, security technology and keyless-entry systems. It can be used in the frequency receiving range of  $f_0 = 868 \text{ MHz}$  to  $870 \text{ MHz}$  or  $f_0 = 902 \text{ MHz}$  to  $928 \text{ MHz}$  for ASK or FSK data transmission. All the statements made below refer to 868.3 MHz and 915.0 MHz applications.

**Figure 1.** System Block Diagram



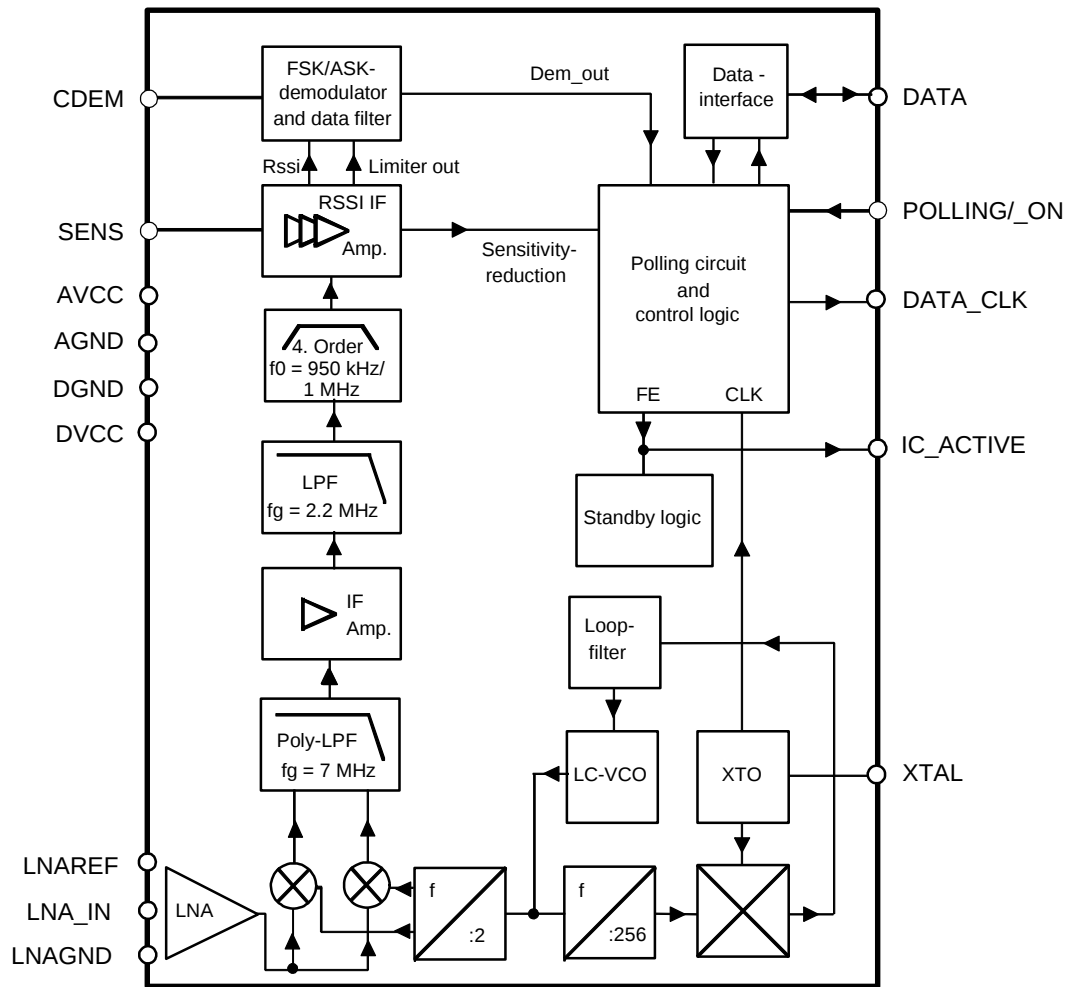
## UHF ASK/FSK Receiver

**T5760/T5761**

**Preliminary**

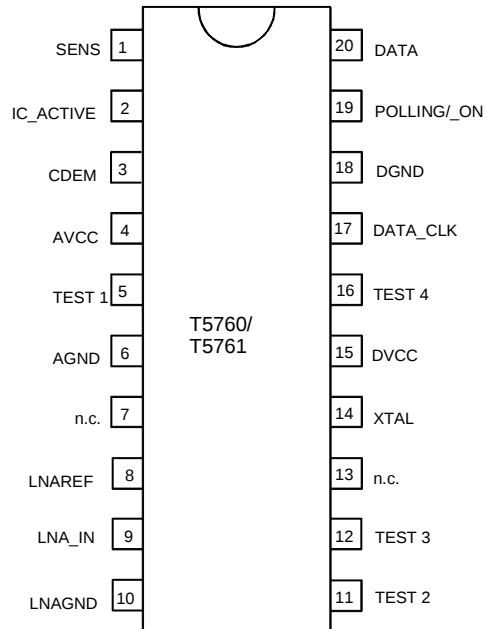


**Figure 2.** Block Diagram



## Pin Configuration

**Figure 3.** Pinning SO20



## Pin Description

| Pin | Symbol      | Function                                                                   |
|-----|-------------|----------------------------------------------------------------------------|
| 1   | SENS        | Sensitivity-control resistor                                               |
| 2   | IC_ACTIVE   | IC condition indicator: Low = sleep mode, High = active mode               |
| 3   | CDEM        | Lower cut-off frequency data filter                                        |
| 4   | AVCC        | Analog power supply                                                        |
| 5   | TEST 1      | Test pin, during operation at GND                                          |
| 6   | AGND        | Analog ground                                                              |
| 7   | n.c.        | Not connected, connect to GND                                              |
| 8   | LNAREF      | High-frequency reference node LNA and mixer                                |
| 9   | LNA_IN      | RF input                                                                   |
| 10  | LNAGND      | DC ground LNA and mixer                                                    |
| 11  | TEST 2      | Do not connect during operating                                            |
| 12  | TEST 3      | Test pin, during operation at GND                                          |
| 13  | n.c.        | Not connected, connect to GND                                              |
| 14  | XTAL        | Crystal oscillator XTAL connection                                         |
| 15  | DVCC        | Digital power supply                                                       |
| 16  | TEST 4      | Test pin, during operation at DVCC                                         |
| 17  | DATA_CLK    | Bit clock of data stream                                                   |
| 18  | DGND        | Digital ground                                                             |
| 19  | POLLING/_ON | Selects polling or receiving mode; Low: receiving mode, High: polling mode |
| 20  | DATA        | Data output/configuration input                                            |

## RF Front End

The RF front end of the receiver is a low-IF heterodyne configuration that converts the input signal into a 950 kHz/1 MHz IF signal with an image rejection of typical 30 dB. According to Figure 3 the front end consists of an LNA (Low Noise Amplifier), LO (Local Oscillator), I/Q mixer, polyphase lowpass filter and an IF amplifier.

The PLL generates the carrier frequency for the mixer via a full integrated synthesizer with integrated low noise LC-VCO (Voltage Controlled Oscillator) and PLL-loop filter. The XTO (crystal oscillator) generates the reference frequency  $f_{XTO}$ . The integrated LC-VCO generates two times the mixer drive frequency  $f_{VCO}$ . The I/Q signals for the mixer are generated with a divide by two circuit ( $f_{LO} = f_{VCO}/2$ ).  $f_{VCO}$  is divided by a factor of 256 and feeds into a phase frequency detector and compared with  $f_{XTO}$ . The output of the phase frequency detector is fed into an integrated loop filter and thereby generates the control voltage for the VCO. If  $f_{LO}$  is determined,  $f_{XTO}$  can be calculated using the following formula:

$$f_{XTO} = f_{LO}/128$$

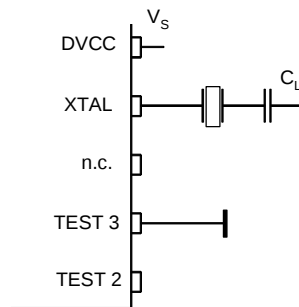
The XTO is a one-pin oscillator that operates at the series resonance of the quartz crystal with high current but low voltage signal, so that there is only a small voltage at the crystal oscillator frequency at Pin XTAL. According to Figure 4, the crystal should be connected to GND with a series capacitor  $C_L$ . The value of that capacitor is recommended by the crystal supplier. Due to a somewhat inductive impedance at steady state oscillation and some PCB parasitics a lower value of  $C_L$  is normally necessary.

The value of  $C_L$  should be optimized for the individual board layout to achieve the exact value of  $f_{XTO}$  (the best way is to use a crystal with known load resonance frequency to find the right value for this capacitor) and hereby of  $f_{LO}$ . When designing the system in terms of receiving bandwidth and local oscillator accuracy, the accuracy of the crystal and the XTO must be considered.

If a crystal with  $\pm 30$  ppm adjustment tolerance at 25°C,  $\pm 50$  ppm over temperature -40°C to +105°C,  $\pm 10$  ppm of total aging and a CM (motional capacitance) of 7 fF is used, an additional XTO pulling of  $\pm 30$  ppm has to be added.

The resulting total LO tolerance of  $\pm 120$  ppm agrees with the receiving bandwidth specification of the T5760/T5761 if the T5750 has also a total LO tolerance of  $\pm 120$  ppm.

**Figure 4.** XTO Peripherals



The nominal frequency  $f_{LO}$  is determined by the RF input frequency  $f_{RF}$  and the IF frequency  $f_{IF}$  using the following formula (low side injection):

$$f_{LO} = f_{RF} - f_{IF}$$

To determine  $f_{LO}$ , the construction of the IF filter must be considered at this point. The nominal IF frequency is  $f_{IF} = 950$  kHz. To achieve a good accuracy of the filter corner frequencies, the filter is tuned by the crystal frequency  $f_{XTO}$ . This means that there is a fixed relation between  $f_{IF}$  and  $f_{LO}$ .

$$f_{IF} = f_{LO}/915$$

The relation is designed to achieve the nominal IF frequency of  $f_{IF} = 950$  kHz for the 868.3 MHz version. For the 915 MHz version an IF frequency of  $f_{IF} = 1.0$  MHz results.

The RF input either from an antenna or from an RF generator must be transformed to the RF input Pin LNA\_IN. The input impedance of that pin is provided in the electrical parameters. The parasitic board inductances and capacitances influence the input matching. The RF receiver T5760/T5761 exhibits its highest sensitivity if the LNA is power matched. This makes the matching to an SAW filter as well as to  $50\ \Omega$  or an antenna easier.

Figure 33 shows a typical input matching network for  $f_{RF} = 868.3$  MHz to  $50\ \Omega$ . Figure 34 illustrates an according input matching for 868.3 MHz to an SAW. The input matching network shown in Figure 33 is the reference network for the parameters given in the electrical characteristics.

## Analog Signal Processing

### IF Filter

The signals coming from the RF front-end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is  $f_{IF} = 950$  kHz for applications where  $f_{RF} = 868.3$  MHz and  $f_{IF} = 1.0$  MHz for  $f_{RF} = 915$  MHz. The nominal bandwidth is 600 kHz.

### Limiting RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is  $DR_{RSSI} = 60$  dB. If the RSSI amplifier is operated within its linear range, the best S/N ratio is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the S/N ratio is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is about 60 dB higher compared to the RF input signal at full sensitivity.

In FSK mode the S/N ratio is not affected by the dynamic range of the RSSI amplifier, because only the hard limited signal from a high gain limiting amplifier is used by the demodulator.

The output voltage of the RSSI amplifier is internally compared to a threshold voltage  $V_{Th\_red}$ .  $V_{Th\_red}$  is determined by the value of the external resistor  $R_{Sens}$ .  $R_{Sens}$  is connected between Pin SENS and GND or  $V_S$ . The output of the comparator is fed into the digital control logic. By this means it is possible to operate the receiver at a lower sensitivity.

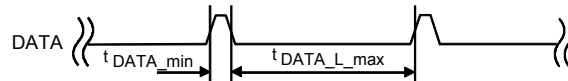
If  $R_{Sens}$  is connected to GND, the receiver switches to full sensitivity. It is also possible to connect the Pin SENS directly to GND to get the maximum sensitivity.

If  $R_{Sens}$  is connected to  $V_S$ , the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of  $R_{Sens}$ , the maximum sensitivity by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is illustrated in Figure 33 and exhibits the best possible sensitivity and at the same time power matching at RF\_IN.

R<sub>Sens</sub> can be connected to V<sub>S</sub> or GND via a microcontroller. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver will not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at Pin DATA will disappear when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern according to Figure 5 is issued at Pin DATA to indicate that the receiver is still active (see Figure 32).

**Figure 5.** Steady L State Limited DATA Output Pattern



## FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set via the bit ASK/\_FSK in the OPMODE register. Logic 'L' sets the demodulator to FSK, applying 'H' to ASK mode.

In ASK mode an automatic threshold control circuit (ATC) is employed to set the detection reference voltage to a value where a good signal to noise ratio is achieved. This circuit also implies the effective suppression of any kind of in-band noise signals or competing transmitters. If the S/N (ratio to suppress in-band noise signals) exceeds about 10 dB the data signal can be detected properly, but better values are found for many modulation schemes of the competing transmitter.

The FSK demodulator is intended to be used for an FSK deviation of  $10 \text{ kHz} \leq \Delta f \leq 100 \text{ kHz}$ . In FSK mode the data signal can be detected if the S/N (ratio to suppress in-band noise signals) exceeds about 2 dB. This value is valid for all modulation schemes of a disturber signal.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the S/N ratio as its passband can be adopted to the characteristics of the data signal. The data filter consists of a 1<sup>st</sup>-order high pass and a 2<sup>nd</sup>-order lowpass filter.

The highpass filter cut-off frequency is defined by an external capacitor connected to Pin CDEM. The cut-off frequency of the highpass filter is defined by the following formula:

$$f_{cu\_DF} = \frac{1}{2 \times \pi \times 30 \text{ k}\Omega \times \text{CDEM}}$$

In self-polling mode, the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the lowpass filter is defined by the selected baud-rate range (BR\_Range). The BR\_Range is defined in the OPMODE register (refer to chapter 'Configuration of the Receiver'). The BR\_Range must be set in accordance to the used baud-rate.

The T5760/T5761 is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of  $V_{DC\_min} = 33\%$  and  $V_{DC\_max} = 66\%$ . The sensitivity may be reduced by up to 2 dB in that condition.

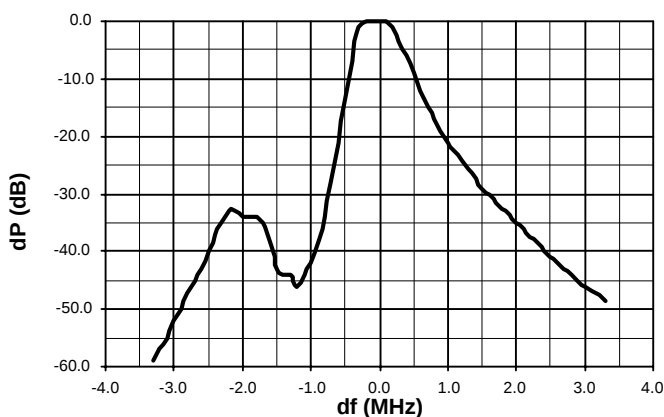
Each BR\_Range is also defined by a minimum and a maximum edge-to-edge time ( $t_{ee\_sig}$ ). These limits are defined in the electrical characteristics. They should not be exceeded to maintain full sensitivity of the receiver.

## Receiving Characteristics

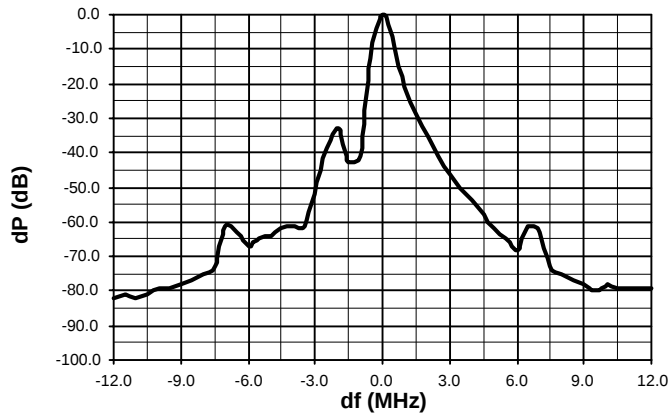
The RF receiver T5760/T5761 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity and large signal capability. The receiving frequency response without a SAW front-end filter is illustrated in Figure 6 and Figure 7. This example relates to ASK mode. FSK mode exhibits a similar behavior. The plots are printed relatively to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 3 dB must be considered, but the overall selectivity is much better.

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated, to be the sum of the deviation of the crystal and the XTO deviation of the T5760/T5761. Low-cost crystals are specified to be within  $\pm 90$  ppm over tolerance, temperature and aging. The XTO deviation of the T5760/T5761 is an additional deviation due to the XTO circuit. This deviation is specified to be  $\pm 30$  ppm worst case for a crystal with  $CM = 7$  fF. If a crystal of  $\pm 90$  ppm is used, the total deviation is  $\pm 120$  ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode but not in FSK mode.

**Figure 6.** Narrow Band Receiving Frequency Response



**Figure 7. Wide Band Receiving Frequency Response**



## Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected, the receiver remains active and transfers the data to the connected microcontroller. If there is no valid signal present, the receiver is in sleep mode most of the time resulting in low current consumption. This condition is called polling mode. A connected microcontroller is disabled during that time.

All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate etc.

Regarding the number of connection wires to the microcontroller, the receiver is very flexible. It can be either operated by a single bi-directional line to save ports to the connected microcontroller or it can be operated by up to five uni-directional ports.

## Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. This clock cycle  $T_{\text{Clk}}$  is derived from the crystal oscillator (XTO) in combination with a divide by 14 circuit. According to chapter 'RF Front End', the frequency of the crystal oscillator ( $f_{\text{XTO}}$ ) is defined by the RF input signal ( $f_{\text{RFIn}}$ ) which also defines the operating frequency of the local oscillator ( $f_{\text{LO}}$ ). The basic clock cycle is  $T_{\text{Clk}} = 14/f_{\text{XTO}}$  giving  $T_{\text{Clk}} = 2.066 \mu\text{s}$  for  $f_{\text{RF}} = 868.3 \text{ MHz}$  and  $T_{\text{Clk}} = 1.961 \mu\text{s}$  for  $f_{\text{RF}} = 915 \text{ MHz}$ .

$T_{\text{Clk}}$  controls the following application-relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency ( $f_{\text{IF0}}$ )

Most applications are dominated by two transmission frequencies:  $f_{\text{Transmit}} = 915 \text{ MHz}$  is mainly used in USA,  $f_{\text{Transmit}} = 868.3 \text{ MHz}$  in Europe. In order to ease the usage of all  $T_{\text{Clk}}$ -dependent parameters on this electrical characteristics display three conditions for each parameter.

- Application USA ( $f_{XTO} = 7.14063 \text{ MHz}$ ,  $T_{Clk} = 1.961 \mu\text{s}$ )
- Application Europe ( $f_{XTO} = 6.77617 \text{ MHz}$ ,  $T_{Clk} = 2.066 \mu\text{s}$ )
- Other applications The electrical characteristic is given as a function of  $T_{Clk}$ .

The clock cycle of some function blocks depends on the selected baud-rate range (BR\_Range) which is defined in the OPMODE register. This clock cycle  $T_{XClk}$  is defined by the following formulas for further reference:

$$\begin{aligned} \text{BR\_Range} = \text{BR\_Range0: } & T_{XClk} = 8 \times T_{Clk} \\ & \text{BR\_Range1: } T_{XClk} = 4 \times T_{Clk} \\ & \text{BR\_Range2: } T_{XClk} = 2 \times T_{Clk} \\ & \text{BR\_Range3: } T_{XClk} = 1 \times T_{Clk} \end{aligned}$$

## Polling Mode

According to Figure 11, the receiver stays in polling mode in a continuous cycle of three different modes. In sleep mode the signal processing circuitry is disabled for the time period  $T_{Sleep}$  while consuming low current of  $I_S = I_{Soff}$ . During the start-up period,  $T_{Startup}$ , all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit by bit contra a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period  $T_{Bit-check}$ . This period varies check by check as it is a statistical process. An average value for  $T_{Bit-check}$  is given in the electrical characteristics. During  $T_{Startup}$  and  $T_{Bit-check}$  the current consumption is  $I_S = I_{Son}$ . The condition of the receiver is indicated on Pin IC\_ACTIVE. The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{Spoll} = \frac{I_{Soff} \times T_{Sleep} + I_{Son} \times (T_{Startup} + T_{Bit-check})}{T_{Sleep} + T_{Startup} + T_{Bit-check}}$$

During  $T_{Sleep}$  and  $T_{Startup}$  the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command the transmitter must start the telegram with an adequate preburst. The required length of the preburst depends on the polling parameters  $T_{Sleep}$ ,  $T_{Startup}$ ,  $T_{Bit-check}$  and the start-up time of a connected microcontroller ( $T_{Start\_microcontroller}$ ). Thus,  $T_{Bit-check}$  depends on the actual bit rate and the number of bits ( $N_{Bit-check}$ ) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{Purburst} \geq T_{Sleep} + T_{Startup} + T_{Bit-check} + T_{Start\_microcontroller}$$

## Sleep Mode

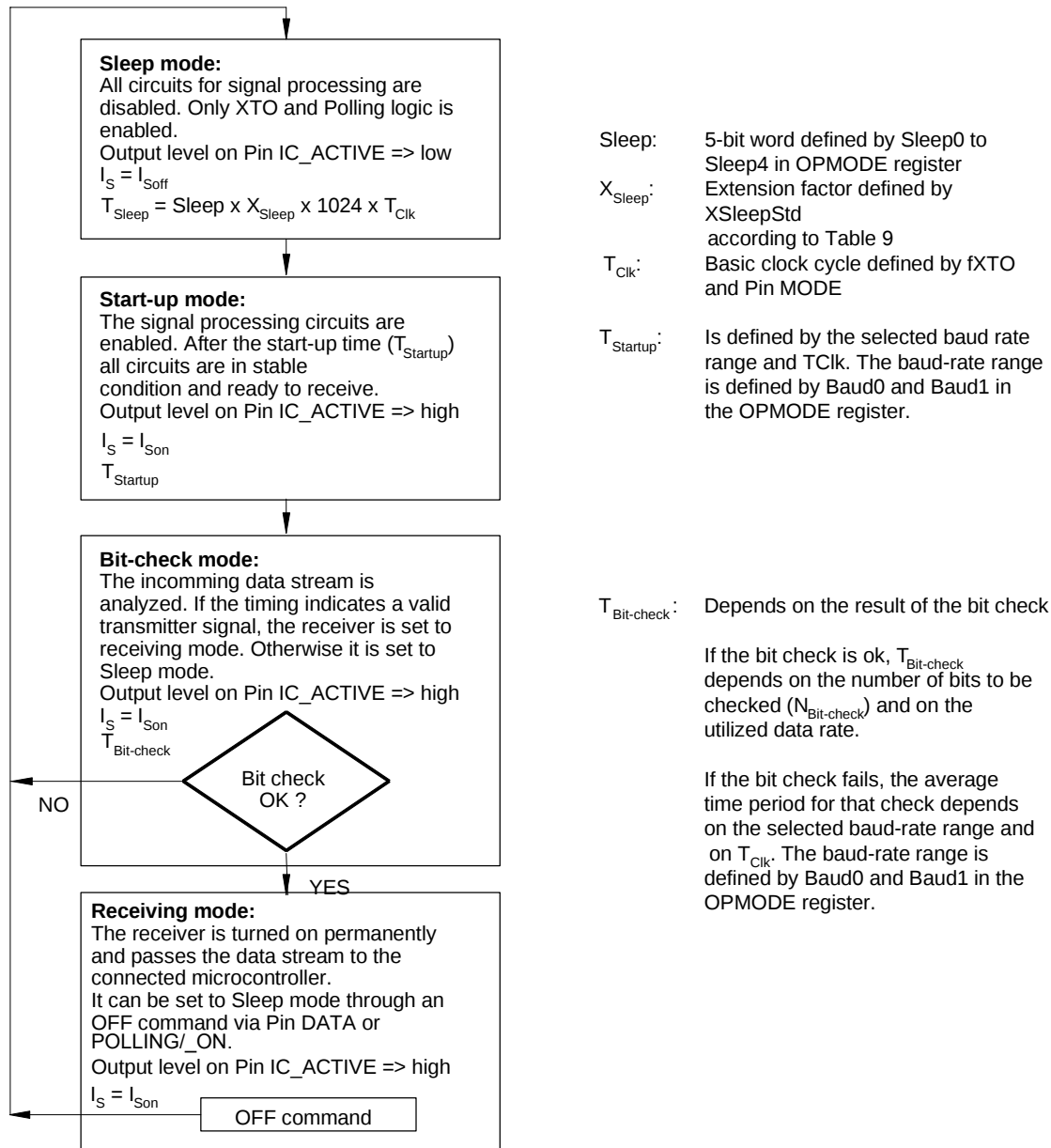
The length of period  $T_{Sleep}$  is defined by the 5-bit word Sleep of the OPMODE register, the extension factor XSleep (according to Table 8), and the basic clock cycle  $T_{Clk}$ . It is calculated to be:

$$T_{Sleep} = \text{Sleep} \times X_{Sleep} \times 1024 \times T_{Clk}$$

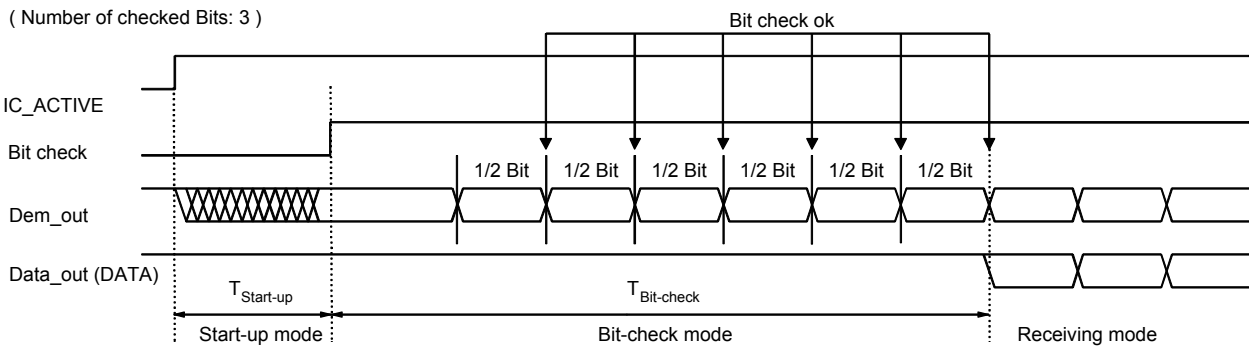
In US- and European applications, the maximum value of  $T_{Sleep}$  is about 60 ms if XSleep is set to 1. The time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting XSleep to 8. XSleep can be set to 8 by bit XSleep<sub>Std</sub> to '1'.

According to Table 7, the highest register value of sleep sets the receiver into a permanent sleep condition. The receiver remains in that condition until another value for Sleep is programmed into the OPMODE register. This function is desirable where several devices share a single data line and may also be used for microcontroller polling – via Pin POLLING/\_ON, the receiver can be switched on and off.

**Figure 8. Polling Mode Flow Chart**



**Figure 9. Timing Diagram for Complete Successful Bit Check**



## Bit-check Mode

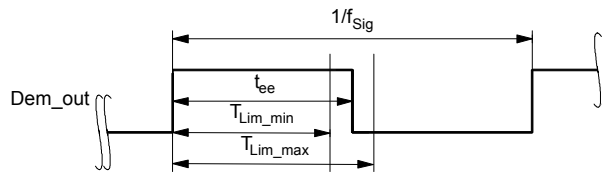
In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distances between 2 signal edges are continuously compared to a programmable time window. The maximum count of this edge-to-edge tests before the receiver switches to receiving mode is also programmable.

## Configuring the Bit Check

Assuming a modulation scheme that contains 2 edges per bit, two time frame checks are verifying one bit. This is valid for Manchester, Bi-phase and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable  $N_{\text{Bit-check}}$  in the OPMODE register. This implies 0, 6, 12 and 18 edge-to-edge checks respectively. If  $N_{\text{Bit-check}}$  is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if  $N_{\text{Bit-check}}$  is set to a lower value. In polling mode, the bit-check time is not dependent on  $N_{\text{Bit-check}}$ . Figure 9 shows an example where 3 bits are tested successfully and the data signal is transferred to Pin DATA.

According to Figure 10, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time  $t_{ee}$  is in between the lower bit-check limit  $T_{\text{Lim\_min}}$  and the upper bit-check limit  $T_{\text{Lim\_max}}$ , the check will be continued. If  $t_{ee}$  is smaller than  $T_{\text{Lim\_min}}$  or  $t_{ee}$  exceeds  $T_{\text{Lim\_max}}$ , the bit check will be terminated and the receiver switches to sleep mode.

**Figure 10.** Valid Time Window for Bit Check



For best noise immunity it is recommended to use a low span between  $T_{\text{Lim\_min}}$  and  $T_{\text{Lim\_max}}$ . This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A '11111...' or a '10101...' sequence in Manchester or Bi-phase is a good choice concerning that advice. A good compromise between receiver sensitivity and susceptibility to noise is a time window of  $\pm 30\%$  regarding the expected edge-to-edge time  $t_{ee}$ . Using pre-burst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below.

$$T_{\text{Lim\_min}} = \text{Lim\_min} \times T_{\text{XClk}}$$

$$T_{\text{Lim\_max}} = (\text{Lim\_max} - 1) \times T_{\text{XClk}}$$

$\text{Lim\_min}$  and  $\text{Lim\_max}$  are defined by a 5-bit word each within the LIMIT register.

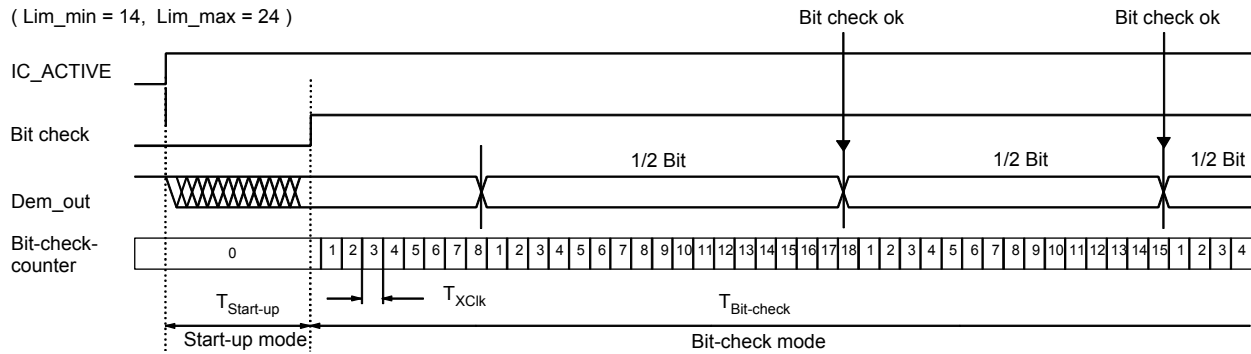
Using above formulas,  $\text{Lim\_min}$  and  $\text{Lim\_max}$  can be determined according to the required  $T_{\text{Lim\_min}}$ ,  $T_{\text{Lim\_max}}$  and  $T_{\text{XClk}}$ . The time resolution defining  $T_{\text{Lim\_min}}$  and  $T_{\text{Lim\_max}}$  is  $T_{\text{XClk}}$ . The minimum edge-to-edge time  $t_{ee}$  ( $t_{\text{DATA\_L\_min}}$ ,  $t_{\text{DATA\_H\_min}}$ ) is defined according to the chapter 'Receiving Mode'. The lower limit should be set to  $\text{Lim\_min} \geq 10$ . The maximum value of the upper limit is  $\text{Lim\_max} = 63$ .

If the calculated value for  $\text{Lim\_min}$  is  $< 19$ , it is recommended to check 6 or 9 bits ( $N_{\text{Bit-check}}$ ) to prevent switching to receiving mode due to noise.

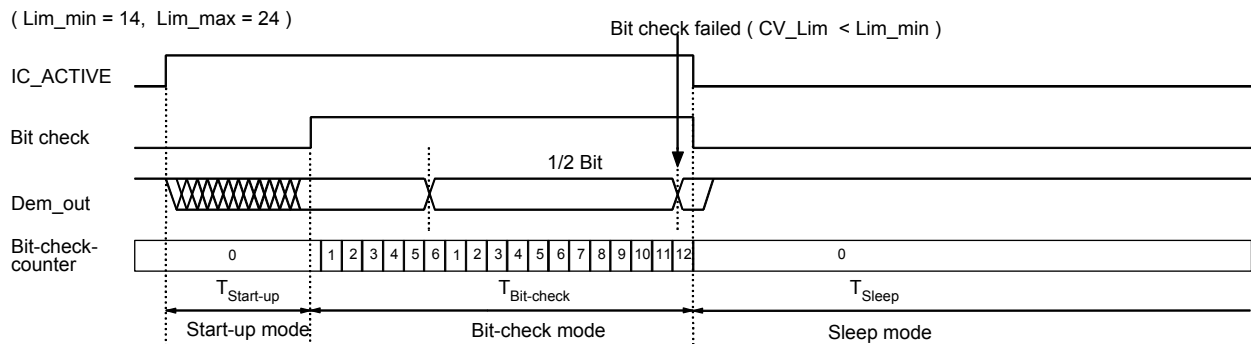
Figure 14, Figure 15 and Figure 16 illustrate the bit check for the bit-check limits  $\text{Lim\_min} = 14$  and  $\text{Lim\_max} = 24$ . When the IC is enabled, the signal processing circuits are enabled during  $T_{\text{Startup}}$ . The output of the ASK/FSK demodulator ( $\text{Dem\_out}$ ) is undefined during that period. When the bit check becomes active, the bit-check counter is clocked with the cycle  $T_{\text{XClk}}$ .

Figure 14 shows how the bit check proceeds if the bit-check counter value  $\text{CV\_Lim}$  is within the limits defined by  $\text{Lim\_min}$  and  $\text{Lim\_max}$  at the occurrence of a signal edge. In Figure 15 the bit check fails as the value  $\text{CV\_Lim}$  is lower than the limit  $\text{Lim\_min}$ . The bit check also fails if  $\text{CV\_Lim}$  reaches  $\text{Lim\_max}$ . This is illustrated in Figure 16.

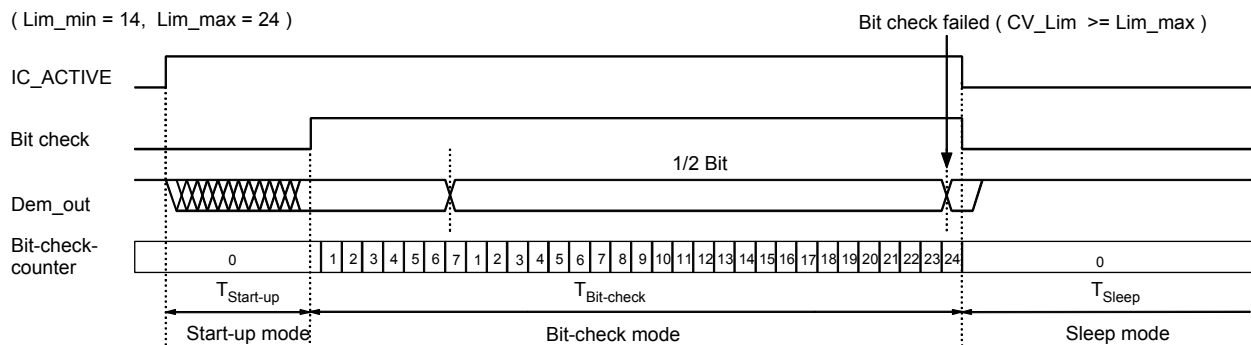
**Figure 11. Timing Diagram During Bit Check**



**Figure 12. Timing Diagram for Failed Bit Check (Condition:  $\text{CV\_Lim} < \text{Lim\_min}$ )**



**Figure 13. Timing Diagram for Failed Bit Check (Condition:  $\text{CV\_Lim} \geq \text{Lim\_max}$ )**



**Duration of the Bit Check** If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and  $T_{\text{Bit-check}}$  varies for each check. Therefore, an average value for  $T_{\text{Bit-check}}$  is given in the electrical characteristics.  $T_{\text{Bit-check}}$  depends on the selected baud-rate range and on  $T_{\text{CLK}}$ . A higher baud-rate range causes a lower value for  $T_{\text{Bit-check}}$  resulting in a lower current consumption in polling mode.

In the presence of a valid transmitter signal,  $T_{\text{Bit-check}}$  is dependent on the frequency of that signal,  $f_{\text{Sig}}$ , and the count of the checked bits,  $N_{\text{Bit-check}}$ . A higher value for  $N_{\text{Bit-check}}$  thereby results in a longer period for  $T_{\text{Bit-check}}$  requiring a higher value for the transmitter pre-burst  $T_{\text{Preburst}}$ .

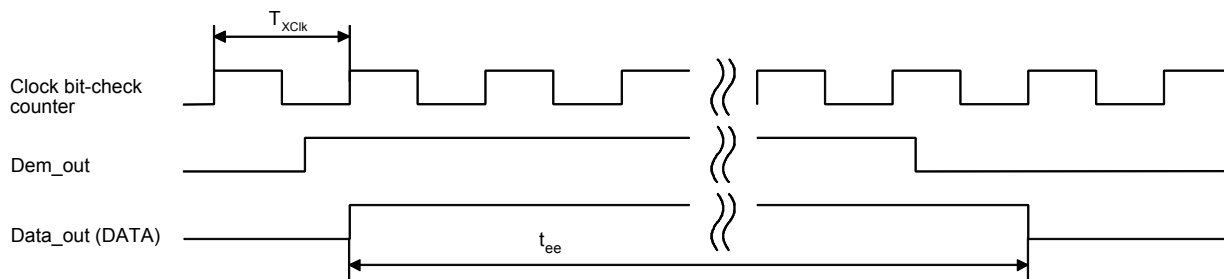
**Receiving Mode** If the bit check was successful for all bits specified by  $N_{\text{Bit-check}}$ , the receiver switches to receiving mode. According to Figure 9, the internal data signal is switched to Pin DATA in that case and the data clock is available after the start bit has been detected (see Figure 20). A connected microcontroller can be woken up by the negative edge at Pin DATA or by the data clock at Pin DATA\_CLK. The receiver stays in that condition until it is switched back to polling mode explicitly.

**Digital Signal Processing** The data from the ASK/FSK demodulator (Dem\_out) is digitally processed in different ways and as a result converted into the output signal data. This processing depends on the selected baud-rate range (BR\_Range). Figure 14 illustrates how Dem\_out is synchronized by the extended clock cycle  $T_{\text{XCLK}}$ . This clock is also used for the bit-check counter. Data can change its state only after  $T_{\text{XCLK}}$  has elapsed. The edge-to-edge time period  $t_{\text{ee}}$  of the Data signal as a result is always an integral multiple of  $T_{\text{XCLK}}$ .

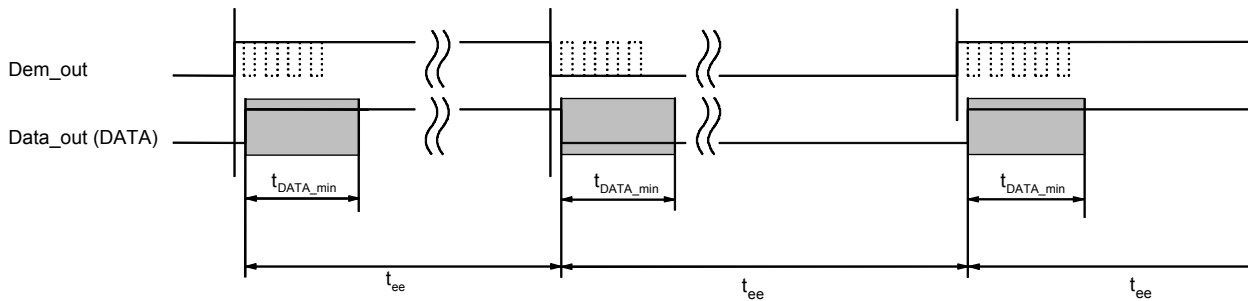
The minimum time period between two edges of the data signal is limited to  $t_{\text{ee}} \geq T_{\text{DATA\_min}}$ . This implies an efficient suppression of spikes at the DATA output. At the same time it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.

The maximum time period for DATA to stay Low is limited to  $T_{\text{DATA\_L\_max}}$ . This function is employed to ensure a finite response time in programming or switching off the receiver via Pin DATA.  $T_{\text{DATA\_L\_max}}$  is thereby longer than the maximum time period indicated by the transmitter data stream. Figure 16 gives an example where Dem\_out remains Low after the receiver has switched to receiving mode.

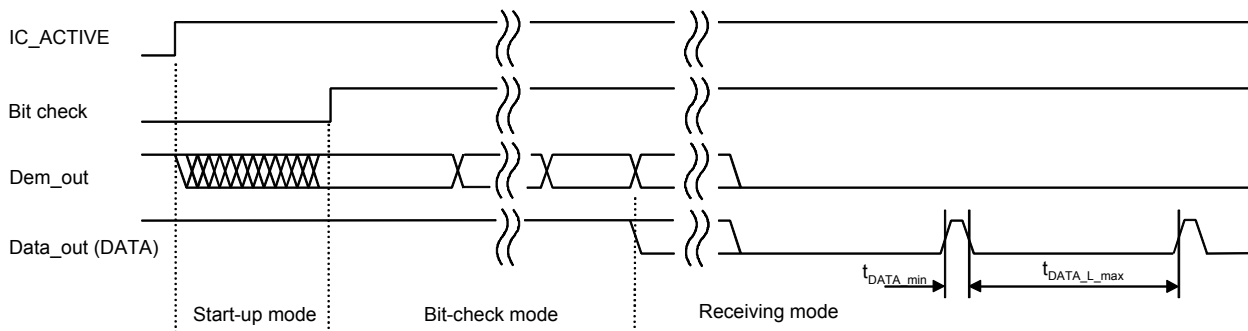
**Figure 14.** Synchronization of the Demodulator Output



**Figure 15.** Debouncing of the Demodulator Output



**Figure 16.** Steady L State Limited DATA Output Pattern After Transmission



After the end of a data transmission, the receiver remains active. Depending of the bit Noise\_Disable in the OPMODE register, the output signal at Pin DATA is high or random noise pulses appear at Pin DATA (see chapter 'Digital Noise Suppression'). The edge-to-edge time period  $t_{ee}$  of the majority of these noise pulses is equal or slightly higher than  $T_{DATA\_min}$ .

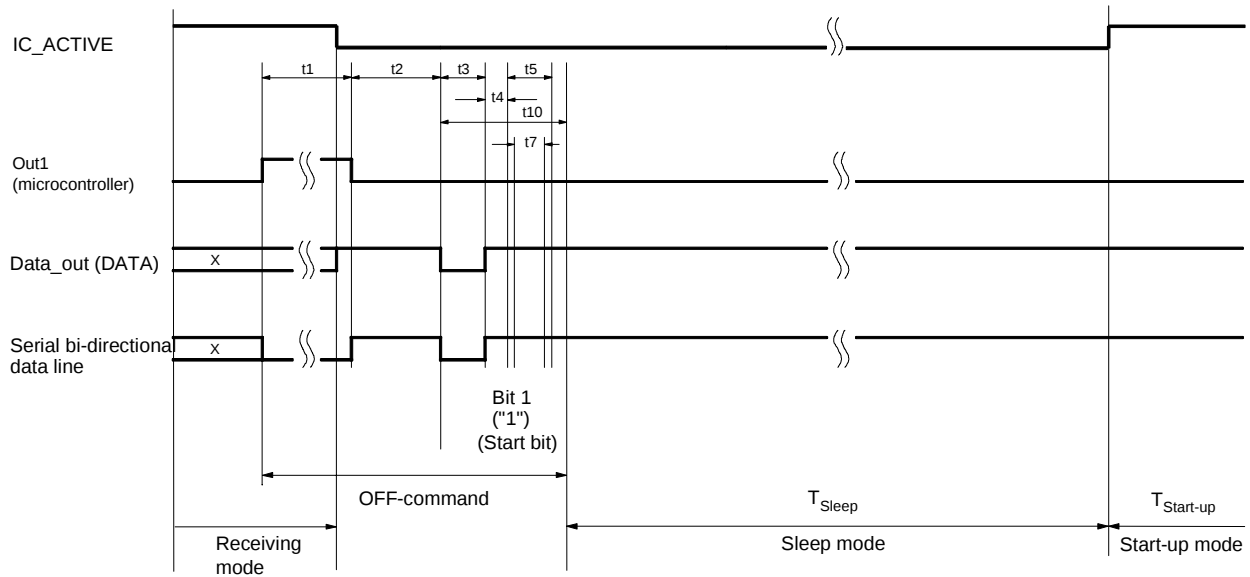
## Switching the Receiver Back to Sleep Mode

The receiver can be set back to polling mode via Pin DATA or via Pin POLLING/\_ON.

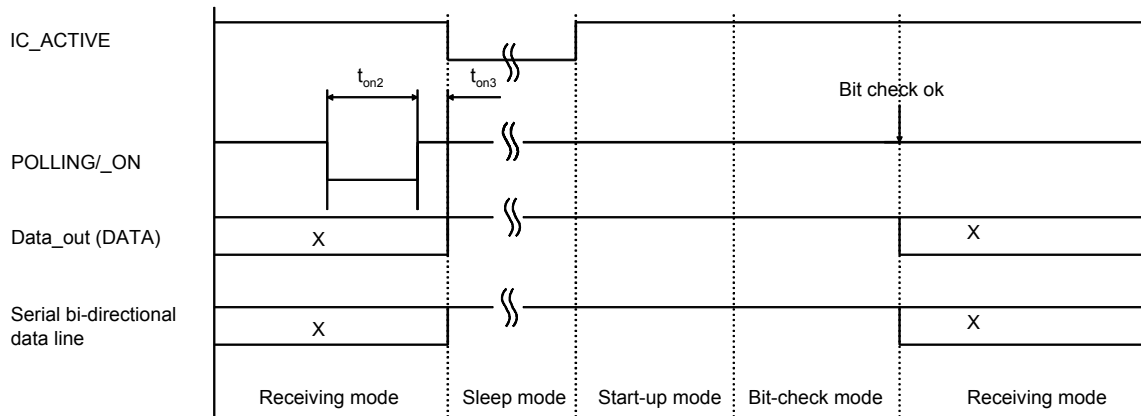
When using Pin DATA, this pin must be pulled to Low for the period  $t_1$  by the connected microcontroller. Figure 17 illustrates the timing of the OFF command (see Figure 32). The minimum value of  $t_1$  depends on BR\_Range. The maximum value for  $t_1$  is not limited but it is recommended not to exceed the specified value to prevent erasing the reset marker. Note also that an internal reset for the OPMODE and the LIMIT register will be generated if  $t_1$  exceeds the specified values. This item is explained in more detail in the chapter 'Configuration of the Receiver'. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 to be '1' during the register configuration. Only one sync pulse ( $t_3$ ) is issued.

The duration of the OFF command is determined by the sum of  $t_1$ ,  $t_2$  and  $t_{10}$ . After the OFF command the sleep time  $T_{Sleep}$  elapses. Note that the capacitive load at Pin DATA is limited (see chapter 'Data Interface').

**Figure 17.** Timing Diagram of the OFF Command via Pin DATA



**Figure 18.** Timing Diagram of the OFF Command via Pin POLLING/\_ON



**Figure 19.** Activating the Receiving Mode via Pin POLLING/\_ON

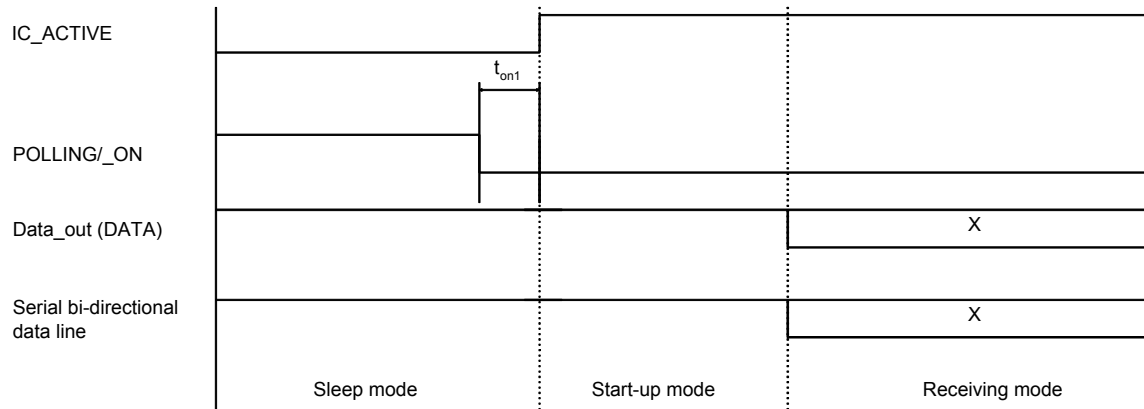


Figure 18 illustrates how to set the receiver back to polling mode via Pin POLLING/\_ON. The Pin POLLING/\_ON must be held to low for the time period  $t_{on2}$ . After the positive edge on Pin POLLING/\_ON and the delay  $t_{on3}$ , the polling mode is active and the sleep time  $T_{Sleep}$  elapses.

This command is faster than using Pin DATA at the cost of an additional connection to the microcontroller.

Figure 19 illustrates how to set the receiver to receiving mode via the Pin POLLING/\_ON. The Pin POLLING/\_ON must be held to Low. After the delay  $t_{on1}$ , the receiver changes from sleep mode to start-up mode regardless the programmed values for  $T_{Sleep}$  and  $N_{Bit-check}$ . As long as POLLING/\_ON is held to Low, the values for  $T_{Sleep}$  and  $N_{Bit-check}$  will be ignored, but not deleted (see chapter 'Digital Noise Suppression').

If the receiver is polled exclusively by a microcontroller,  $T_{Sleep}$  must be programmed to 31 (permanent sleep mode). In this case the receiver remains in sleep mode as long as POLLING/\_ON is held to High.

## Data Clock

The Pin DATA\_CLK makes a data shift clock available to sample the data stream into a shift register. Using this data clock, a microcontroller can easily synchronize the data stream. This clock can only be used for Manchester and Bi-phase coded signals.

### Generation of the Data Clock

After a successful bit check, the receiver switches from polling mode to receiving mode and the data stream is available at Pin DATA. In receiving mode, the data clock control logic (Manchester/Bi-phase demodulator) is active and examines the incoming data stream. This is done, like in the bit check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window. As illustrated in Figure 20, only two distances between two edges in Manchester and Bi-phase coded signals are valid (T and 2T).

The limits for T are the same as used for the bit check. They can be programmed in the LIMIT-register (Lim\_min and Lim\_max, see Table 10 and Table 11).

The limits for 2T are calculated as follows:

Lower limit of 2T:  $Lim\_min\_2T = (Lim\_min + Lim\_max) - (Lim\_max - Lim\_min)/2$

Upper limit of 2T:  $Lim\_max\_2T = (Lim\_min + Lim\_max) + (Lim\_max - Lim\_min)/2$

(If the result for 'Lim\_min\_2T' or 'Lim\_max\_2T' is not an integer value, it will be round up)

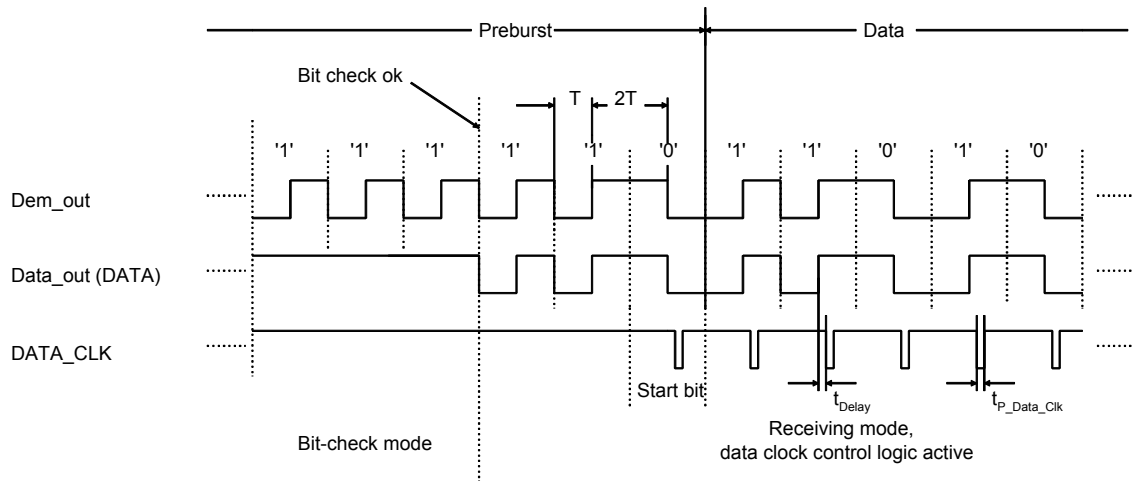
The data clock is available, after the data clock control logic has detected the distance 2T (Start bit) and is issued with the delay  $t_{Delay}$  after the edge on Pin DATA (see Figure 20).

If the data clock control logic detects a timing or logical error (Manchester code violation), like illustrated in Figure 21 and Figure 22, it stops the output of the data clock. The receiver remains in receiving mode and starts with the bit check. If the bit check was successful and the start bit has been detected, the data clock control logic starts again with the generation of the data clock (see Figure 23).

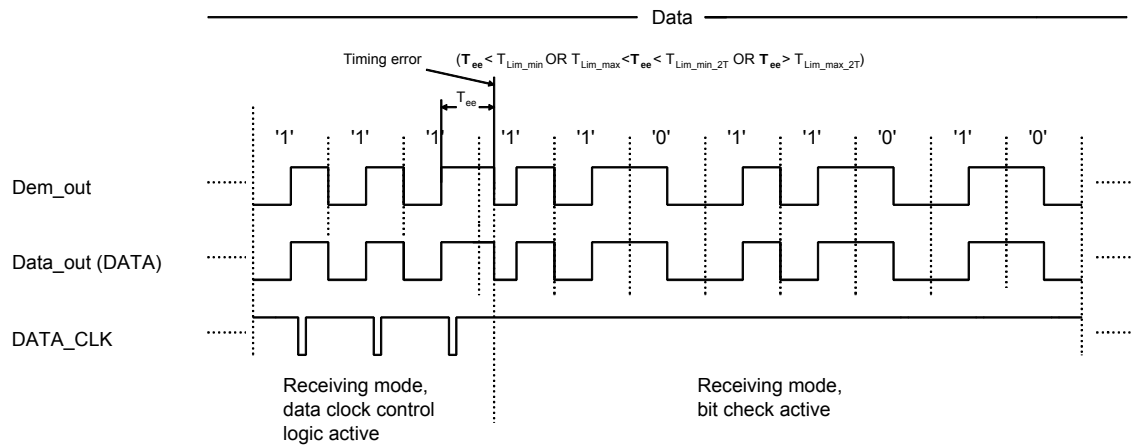
It is recommended to use the function of the data clock only in conjunction with the bit check 3, 6 or 9. If the bit check is set to 0 or the receiver is set to receiving mode via the Pin POLLING/\_ON, the data clock is available if the data clock control logic has detected the distance 2T (Start bit).

Note that for Bi-phase-coded signals, the data clock is issued at the end of the bit.

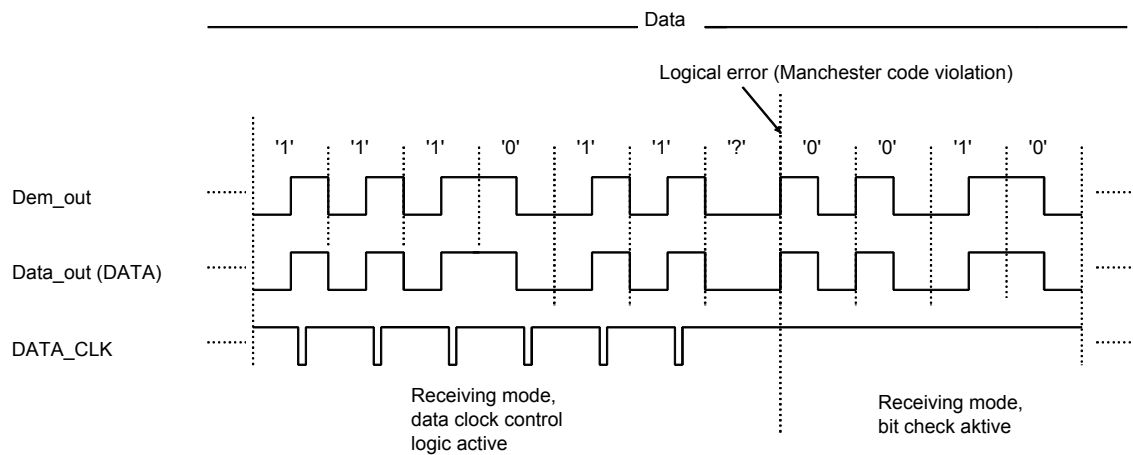
**Figure 20.** Timing Diagram of the Data Clock



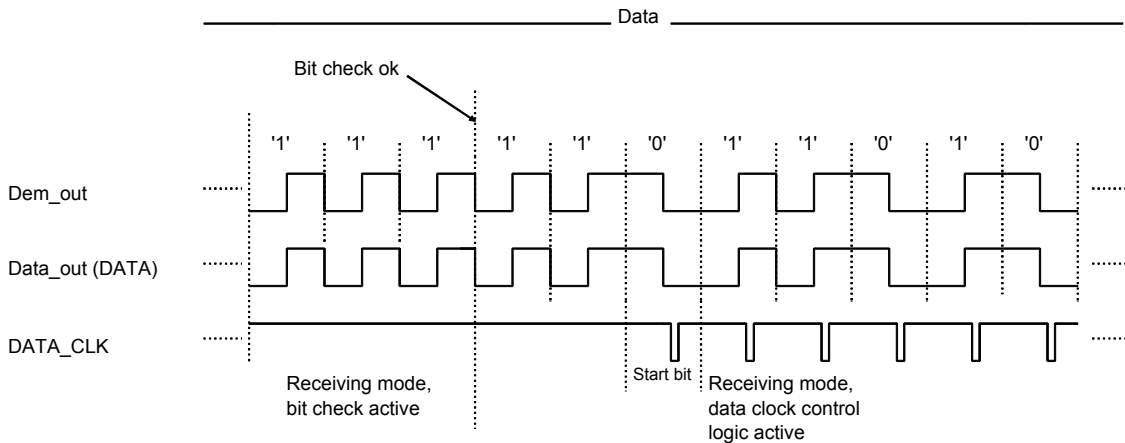
**Figure 21.** Data Clock Disappears Because of a Timing Error



**Figure 22.** Data Clock Disappears Because of a Logical Error



**Figure 23.** Output of the Data Clock After a Successful Bit Check

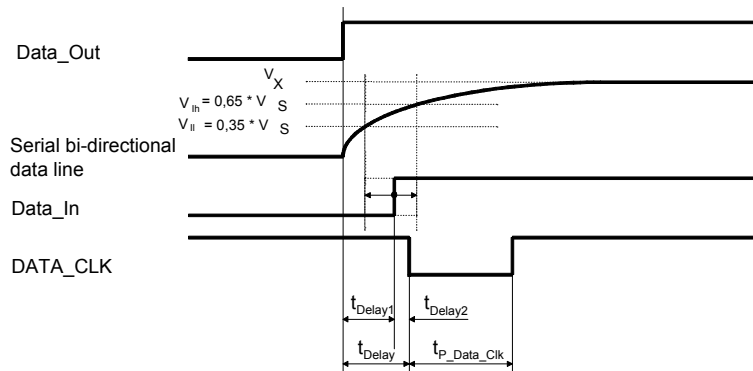


The delay of the data clock is calculated as follows:  $t_{\text{Delay}} = t_{\text{Delay1}} + t_{\text{Delay2}}$

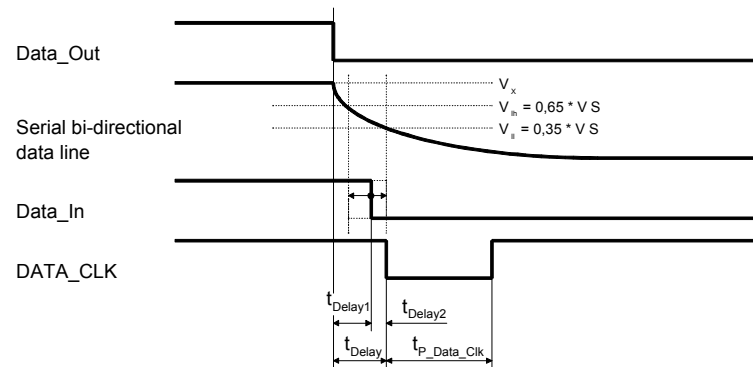
$t_{\text{Delay1}}$  is the delay between the internal signals Data\_Out and Data\_In. For the rising edge,  $t_{\text{Delay1}}$  depends on the capacitive load  $C_L$  at Pin DATA and the external pull-up resistor  $R_{\text{pup}}$ . For the falling edge,  $t_{\text{Delay1}}$  depends additionally on the external voltage  $V_X$  (see Figure 24, Figure 25 and Figure 32). When the level of Data\_In is equal to the level of Data\_Out, the data clock is issued after an additional delay  $t_{\text{Delay2}}$ .

Note that the capacitive load at Pin DATA is limited. If the maximum tolerated capacitive load at Pin DATA is exceeded, the data clock disappears (see chapter 'Data Interface').

**Figure 24.** Timing Characteristic of the Data Clock (Rising Edge on Pin DATA)



**Figure 25.** Timing Characteristic of the Data Clock (Falling Edge of the Pin DATA)



## Digital Noise Suppression

After a data transmission, digital noise appears on the data output (see Figure 26). Preventing that digital noise keeps the connected microcontroller busy. It can be suppressed in two different ways.

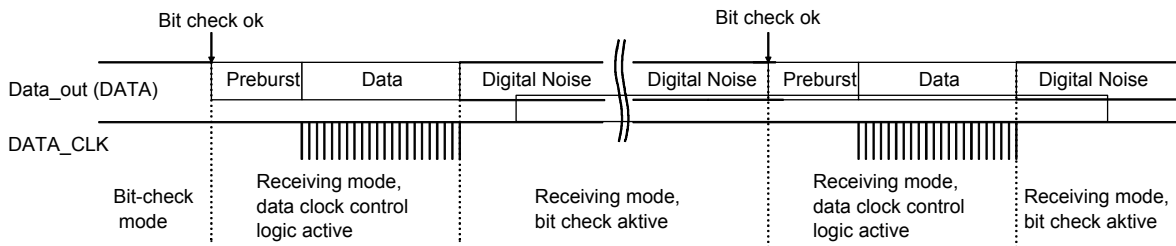
## Automatic Noise Suppression

If the bit Noise\_Disable (Table 9) in the OPMODE register is set to 1 (default), the receiver changes to bit-check mode at the end of a valid data stream. The digital noise is suppressed and the level at Pin DATA is High in that case. The receiver changes back to receiving mode, if the bit check was successful.

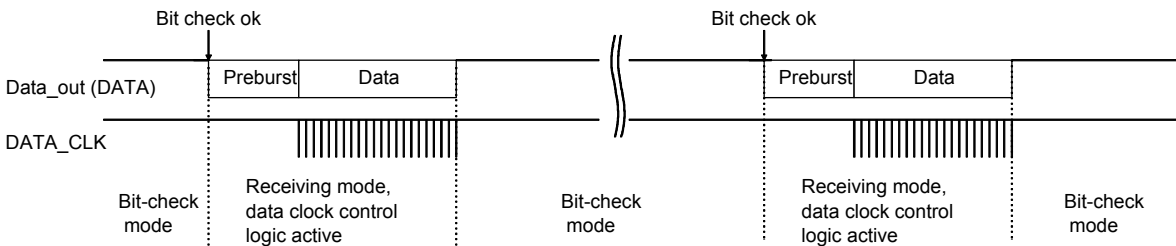
This way to suppress the noise is recommended if the data stream is Manchester or Bi-phase coded and is active after power on.

Figure 28 illustrates the behavior of the data output at the end of a data stream. Note that if the last period of the data stream is a high period (rising edge to falling edge), a pulse occurs on Pin DATA. The length of the pulse depends on the selected baud-rate range.

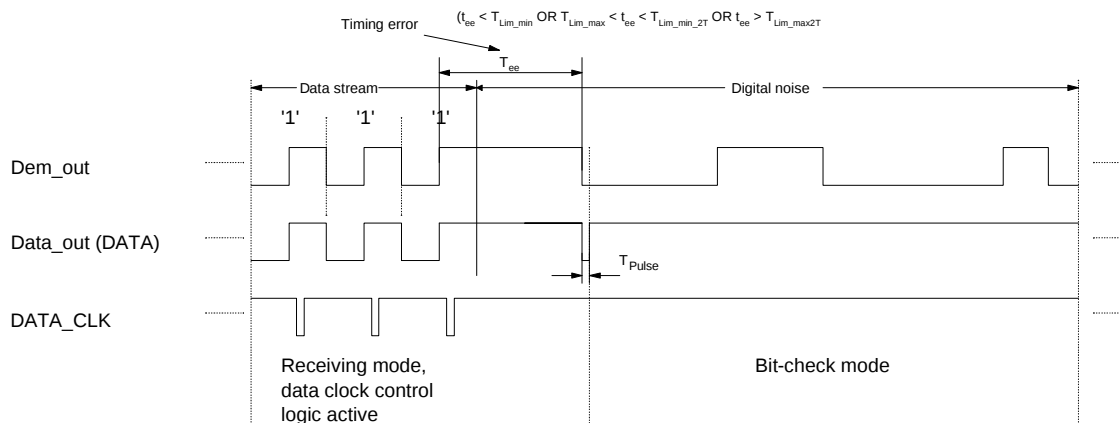
**Figure 26.** Output of Digital Noise at the End of the Data Stream



**Figure 27.** Automatic Noise Suppression

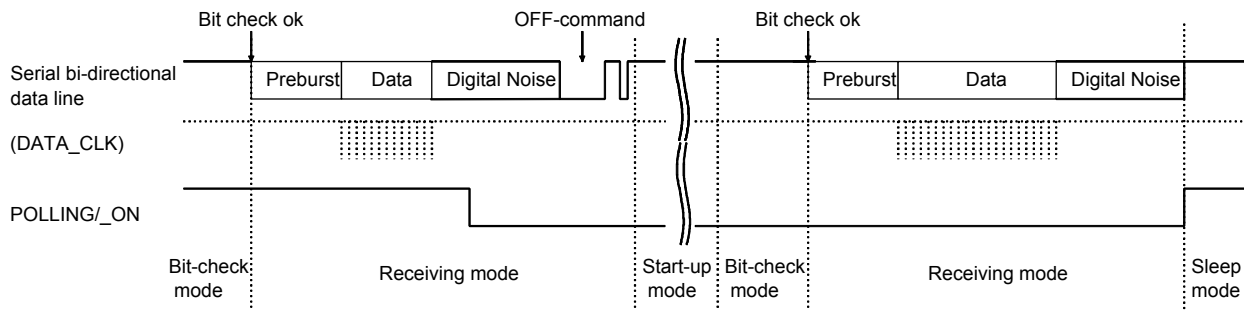


**Figure 28.** Occurrence of a Pulse at the End of the Data Stream



## Controlled Noise Suppression by the Microcontroller

**Figure 29.** Controlled Noise Suppression



If the bit Noise\_Disable (see Table 9) in the OPMODE register is set to 0, digital noise appears at the end of a valid data stream. To suppress the noise, the Pin POLLING/\_ON must be set to Low. The receiver remains in receiving mode. Then, the OFF command causes the change to the start-up mode. The programmed sleep time (see Table 7) will not be executed because the level at Pin POLLING/\_ON is low, but the bit check is active in that case. The OFF command activates the bit check also if the Pin POLLING/\_ON is held to Low. The receiver changes back to receiving mode if the bit check was successful. To activate the polling mode at the end of the data transmission, the Pin POLLING/\_ON must be set to High. This way of suppressing the noise is recommended if the data stream is not Manchester or Bi-phase coded.

## Configuration of the Receiver

The T5760/T5761 receiver is configured via two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bidirectional DATA port. If the register contents have changed due to a voltage drop, this condition is indicated by a certain output pattern called reset marker (RM). The receiver must be reprogrammed in that case. After a Power-On Reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers. Table 3 shows the structure of the registers. According to Table 2, bit 1 defines if the receiver is set back to polling mode via the OFF command (see chapter 'Receiving Mode') or if it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed. To get a high programming reliability, Bit 15 (Stop bit), at the end of the programming operation, must be set to 0.

**Table 1.** Effect of Bit 1 and Bit 2 on Programming the Registers

| Bit 1 | Bit 2 | Action                                                 |
|-------|-------|--------------------------------------------------------|
| 1     | x     | The receiver is set back to polling mode (OFF command) |
| 0     | 1     | The OPMODE register is programmed                      |
| 0     | 0     | The LIMIT register is programmed                       |

**Table 2.** Effect of Bit 15 on Programming the Register

| Bit 15 | Action                                                         |
|--------|----------------------------------------------------------------|
| 0      | The values will be written into the register (OPMODE or LIMIT) |
| 1      | The values will not be written into the register               |

**Table 3.** Effect of the Configuration Words within the Registers

| Bit 1                              | Bit 2 | Bit 3           | Bit 4    | Bit 5                  | Bit 6    | Bit 7           | Bit 8    | Bit 9    | Bit 10   | Bit 11   | Bit 12   | Bit 13                    | Bit 14                    | Bit 15 |
|------------------------------------|-------|-----------------|----------|------------------------|----------|-----------------|----------|----------|----------|----------|----------|---------------------------|---------------------------|--------|
| OFF command                        |       |                 |          |                        |          |                 |          |          |          |          |          |                           |                           |        |
| 1                                  | –     | –               | –        | –                      | –        | –               | –        | –        | –        | –        | –        | –                         | –                         | –      |
| –                                  |       | OPMODE register |          |                        |          |                 |          |          |          |          |          |                           |                           | –      |
| 0                                  | 1     | BR_Range        |          | N <sub>Bit-check</sub> |          | Modu-<br>lation | Sleep    |          |          |          |          | X<br>Sleep                | Noise<br>Suppres-<br>sion | 0      |
|                                    |       | Baud1           | Baud0    | BitChk1                | BitChk0  | ASK/<br>_FSK    | Sleep4   | Sleep3   | Sleep2   | Sleep1   | Sleep0   | X <sub>Sleep</sub><br>Std | Noise_<br>Disable         |        |
| Default<br>values of<br>Bit 3...14 |       | 0               | 0        | 0                      | 1        | 0               | 0        | 0        | 1        | 1        | 0        | 0                         | 1                         | –      |
| –                                  |       | LIMIT register  |          |                        |          |                 |          |          |          |          |          |                           |                           | –      |
| 0                                  | 0     | Lim_min         |          |                        |          |                 |          | Lim_max  |          |          |          |                           |                           | –      |
|                                    |       | Lim_min5        | Lim_min4 | Lim_min3               | Lim_min2 | Lim_min1        | Lim_min0 | Lim_max5 | Lim_max4 | Lim_max3 | Lim_max2 | Lim_max1                  | Lim_max0                  | 0      |
| Default<br>values of<br>Bit 3...14 |       | 0               | 1        | 0                      | 1        | 0               | 1        | 1        | 0        | 1        | 0        | 0                         | 1                         | –      |

The following tables illustrate the effect of the individual configuration words. The default configuration is highlighted for each word.

BR\_Range sets the appropriate baud-rate range and simultaneously defines XLim. XLim is used to define the bit-check limits  $T_{Lim\_min}$  and  $T_{Lim\_max}$  as shown in Table 10 and Table 11.

**Table 4.** Effect of the configuration word BR\_Range

| BR_Range |       | Baud-rate Range/Extension Factor for Bit-check Limits (XLim)                                    |
|----------|-------|-------------------------------------------------------------------------------------------------|
| Baud1    | Baud0 |                                                                                                 |
| 0        | 0     | BR_Range0<br>(application USA/Europe: BR_Range0 = 1.0 kBaud to 1.8 kBaud)<br>XLim = 8 (default) |
| 0        | 1     | BR_Range1<br>(application USA/Europe: BR_Range1 = 1.8 kBaud to 3.2 kBaud)<br>XLim = 4           |
| 1        | 0     | BR_Range2<br>(application USA/Europe: BR_Range2 = 3.2 kBaud to 5.6 kBaud)<br>XLim = 2           |
| 1        | 1     | BR_Range3<br>(Application USA/Europe: BR_Range3 = 5.6 kBaud to 10 kBaud)<br>XLim = 1            |

**Table 5.** Effect of the Configuration word N<sub>Bit-check</sub>

| N <sub>Bit-check</sub> |         | Number of Bits to be Checked |
|------------------------|---------|------------------------------|
| BitChk1                | BitChk0 |                              |
| 0                      | 0       | 0                            |
| 0                      | 1       | 3 (default)                  |
| 1                      | 0       | 6                            |
| 1                      | 1       | 9                            |

**Table 6.** Effect of the Configuration Bit Modulation

| Modulation | Selected Modulation |
|------------|---------------------|
| ASK/_FSK   | —                   |
| 0          | FSK (default)       |
| 1          | ASK                 |

**Table 7.** Effect of the Configuration Word Sleep

| Sleep  |        |        |        |        | Start Value for Sleep Counter<br>( $T_{\text{Sleep}} = \text{Sleep} \times \text{XSleep} \times 1024 \times T_{\text{Clk}}$ )                  |
|--------|--------|--------|--------|--------|------------------------------------------------------------------------------------------------------------------------------------------------|
| Sleep4 | Sleep3 | Sleep2 | Sleep1 | Sleep0 |                                                                                                                                                |
| 0      | 0      | 0      | 0      | 0      | 0 (Receiver is continuously polling until a valid signal occurs)                                                                               |
| 0      | 0      | 0      | 0      | 1      | 1 ( $T_{\text{Sleep}} \approx 2.1$ ms for $\text{XSleep} = 1$ and $f_{\text{RF}} = 868.3$ MHz, $\approx 2.0$ ms for $f_{\text{RF}} = 915$ MHz) |
| 0      | 0      | 0      | 1      | 0      | 2                                                                                                                                              |
| 0      | 0      | 0      | 1      | 1      | 3                                                                                                                                              |
| ...    | ...    | ...    | ...    | ...    | ...                                                                                                                                            |
| 0      | 0      | 1      | 1      | 0      | 6 ( $T_{\text{Sleep}} = 12.695$ ms for $f_{\text{RF}} = 868.3$ MHz, $12.047$ ms for $f_{\text{RF}} = 915$ MHz) (default)                       |
| ...    | ...    | ...    | ...    | ...    | ...                                                                                                                                            |
| 1      | 1      | 1      | 0      | 1      | 29                                                                                                                                             |
| 1      | 1      | 1      | 1      | 0      | 30                                                                                                                                             |
| 1      | 1      | 1      | 1      | 1      | 31 (permanent sleep mode)                                                                                                                      |

**Table 8.** Effect of the Configuration Bit XSleep

| XSleep                       | Extension Factor for Sleep Time<br>( $T_{\text{Sleep}} = \text{Sleep} \times \text{XSleep} \times 1024 \times T_{\text{Clk}}$ ) |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------------|
| $\text{XSleep}_{\text{Std}}$ |                                                                                                                                 |
| 0                            | 1 (default)                                                                                                                     |
| 1                            | 8                                                                                                                               |

**Table 9.** Effect of the Configuration Bit Noise Suppression

| Noise Suppression | Suppression of the Digital Noise at Pin DATA |
|-------------------|----------------------------------------------|
| Noise_Disable     |                                              |
| 0                 | Noise suppression is inactive                |
| 1                 | Noise suppression is active (default)        |

**Table 10.** Effect of the Configuration Word Lim\_min

| Lim_min <sup>(1)</sup> (Lim_min < 10 is not Applicable) |          |          |          |          |          | Lower Limit Value for Bit Check                                                                                                                         |
|---------------------------------------------------------|----------|----------|----------|----------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| Lim_min5                                                | Lim_min4 | Lim_min3 | Lim_min2 | Lim_min1 | Lim_min0 | ( $T_{Lim\_min} = Lim\_min \times XLim \times T_{Clk}$ )                                                                                                |
| 0                                                       | 0        | 1        | 0        | 1        | 0        | 10                                                                                                                                                      |
| 0                                                       | 0        | 1        | 0        | 1        | 1        | 11                                                                                                                                                      |
| 0                                                       | 0        | 1        | 1        | 0        | 0        | 12                                                                                                                                                      |
| ..                                                      | ..       | ..       | ..       | ..       | ..       |                                                                                                                                                         |
| 0                                                       | 1        | 0        | 1        | 0        | 1        | 21 (default)<br>( $T_{Lim\_min} = 347 \mu s$ for $f_{RF} = 868.3$ MHz and BR_Range0<br>$T_{Lim\_min} = 329 \mu s$ for $f_{RF} = 915$ MHz and BR_Range0) |
| ..                                                      | ..       | ..       | ..       | ..       | ..       |                                                                                                                                                         |
| 1                                                       | 1        | 1        | 1        | 0        | 1        | 61                                                                                                                                                      |
| 1                                                       | 1        | 1        | 1        | 1        | 0        | 62                                                                                                                                                      |
| 1                                                       | 1        | 1        | 1        | 1        | 1        | 63                                                                                                                                                      |

Note: 1. Lim\_min is also used to determine the margins of the data clock control logic (see chapter 'Data Clock').

**Table 11.** Effect of the Configuration Word Lim\_max

| Lim_max <sup>(1)</sup> (Lim_max < 12 is not applicable) |          |          |          |          |          | Upper Limit Value for Bit Check                                                                                                                 |
|---------------------------------------------------------|----------|----------|----------|----------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| Lim_max5                                                | Lim_max4 | Lim_max3 | Lim_max2 | Lim_max1 | Lim_max0 | ( $TLim\_max = (Lim\_max - 1) \times XLim \times T_{Clk}$ )                                                                                     |
| 0                                                       | 0        | 1        | 1        | 0        | 0        | 12                                                                                                                                              |
| 0                                                       | 0        | 1        | 1        | 0        | 1        | 13                                                                                                                                              |
| 0                                                       | 0        | 1        | 1        | 1        | 0        | 14                                                                                                                                              |
| ..                                                      | ..       | ..       | ..       | ..       | ..       |                                                                                                                                                 |
| 1                                                       | 0        | 1        | 0        | 0        | 1        | 41 (default)<br>( $TLim\_max = 661 \mu s$ for $f_{RF} = 868.3$ MHz and BR_Range0, $TLim\_max = 627 \mu s$ for $f_{RF} = 915$ MHz and BR_Range0) |
| ..                                                      | ..       | ..       | ..       | ..       | ..       |                                                                                                                                                 |
| 1                                                       | 1        | 1        | 1        | 0        | 1        | 61                                                                                                                                              |
| 1                                                       | 1        | 1        | 1        | 1        | 0        | 62                                                                                                                                              |
| 1                                                       | 1        | 1        | 1        | 1        | 1        | 63                                                                                                                                              |

Note: 1. Lim\_max is also used to determine the margins of the data clock control logic (see chapter 'Data Clock').

## Conservation of the Register Information

The T5760/T5761 implies an integrated power-on reset and brown-out detection circuitry to provide a mechanism to preserve the RAM register information.

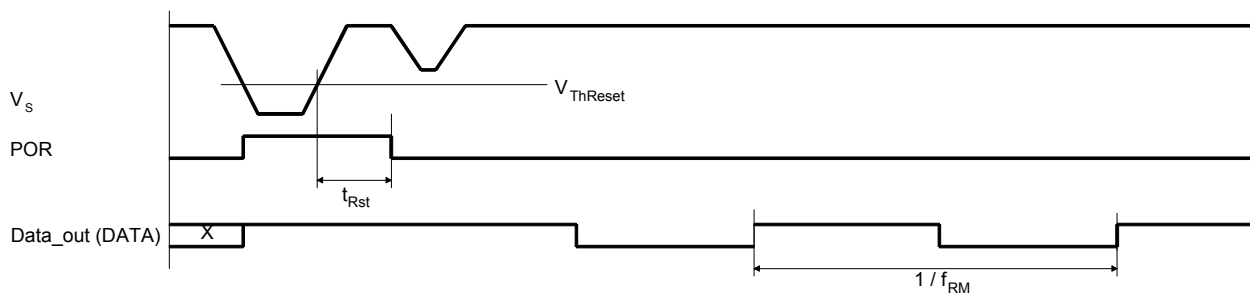
According to Figure 30, a power-on reset (POR) is generated if the supply voltage  $V_S$  drops below the threshold voltage  $V_{ThReset}$ . The default parameters are programmed into the configuration registers in that condition. Once  $V_S$  exceeds  $V_{ThReset}$  the POR is canceled after the minimum reset period  $t_{Rst}$ . A POR is also generated when the supply voltage of the receiver is turned on.

To indicate that condition, the receiver displays a reset marker (RM) at Pin DATA after a reset. The RM is represented by the fixed frequency  $f_{RM}$  at a 50% duty-cycle. RM can be canceled via a Low pulse  $t_1$  at Pin DATA. The RM implies the following characteristics:

- $f_{RM}$  is lower than the lowest feasible frequency of a data signal. By this means, RM cannot be misinterpreted by the connected microcontroller.
- If the receiver is set back to polling mode via Pin DATA, RM cannot be canceled by accident if  $t_1$  is applied according to the proposal in the section “Programming the Configuration Registers”.

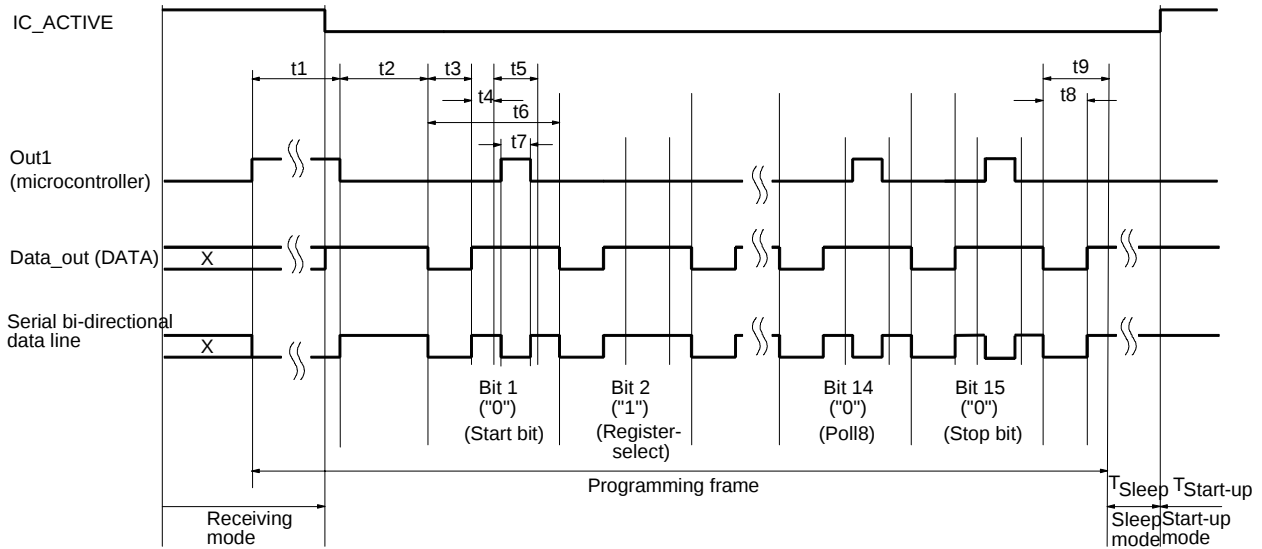
By means of that mechanism the receiver cannot lose its register information without communicating that condition via the reset marker RM.

**Figure 30.** Generation of the Power-on Reset

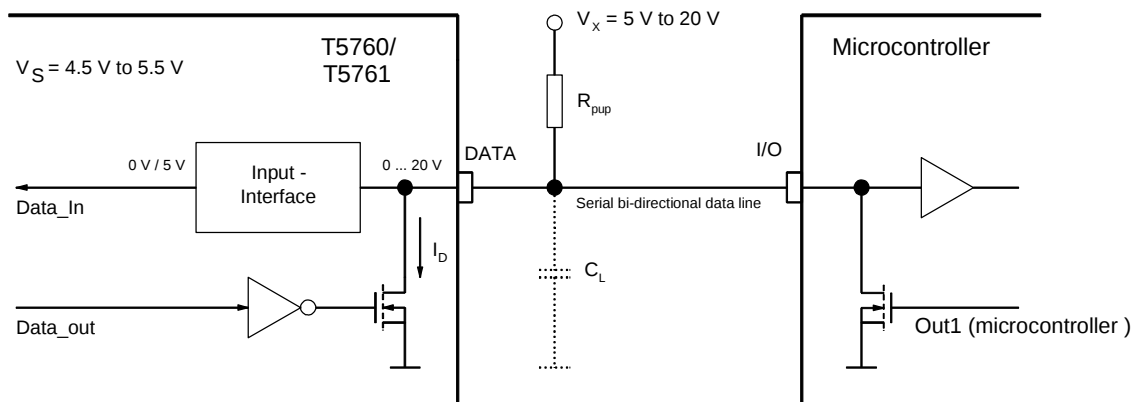


## Programming the Configuration Register

**Figure 31.** Timing of the Register Programming



**Figure 32.** Data Interface



The configuration registers are programmed serially via the bi-directional data line according to Figure 31 and Figure 32.

To start programming, the serial data line DATA is pulled to Low for the time period t1 by the microcontroller. When DATA has been released, the receiver becomes the master device. When the programming delay period t2 has elapsed, it emits 15 subsequent synchronization pulses with the pulse length t3. After each of these pulses, a programming window occurs. The delay until the program window starts is determined by t4, the duration is defined by t5. Within the programming window, the individual bits are set. If the microcontroller pulls down Pin DATA for the time period t7 during t5, the according bit is set to '0'. If no programming pulse t7 is issued, this bit is set to '1'. All 15 bits are subsequently programmed this way. The time frame to program a bit is defined by t6.

Bit 15 is followed by the equivalent time window  $t_9$ . During this window, the equivalence acknowledge pulse  $t_8$  (E\_Ack) occurs if the just programmed mode word is equivalent to the mode word that was already stored in that register. E\_Ack should be used to verify that the mode word was correctly transferred to the register. The register must be programmed twice in that case.

Programming of a register is possible both in sleep-mode and in active-mode of the receiver.

During programming, the LNA, LO, lowpass filter IF-amplifier and the FSK/ASK Manchester demodulator are disabled.

The programming start pulse  $t_1$  initiates the programming of the configuration registers. If bit 1 is set to '1', it represents the OFF command to set the receiver back to polling mode at the same time. For the length of the programming start pulse  $t_1$ , the following convention should be considered:

- $t_1(\min) < t_1 < 5632 T_{\text{Clk}}$ :  
 $t_1(\min)$  is the minimum specified value for the relevant BR\_Range

Programming respectively OFF command is initiated if the receiver is not in reset mode. If the receiver is in reset mode, programming respectively Off command is not initiated and the reset marker RM is still present at Pin DATA.

This period is generally used to switch the receiver to polling mode or to start the programming of a register. In reset condition, RM is not cancelled by accident.

- $t_1 > 7936 \times T_{\text{Clk}}$

Programming respectively OFF command is initiated in any case. The registers OPMODE and LIMIT are set to the default values. RM is cancelled if present.

This period is used if the connected microcontroller detected RM. If the receiver operates in default mode, this time period for  $t_1$  can generally be used.

Note that the capacitive load at Pin DATA is limited.

## Data Interface

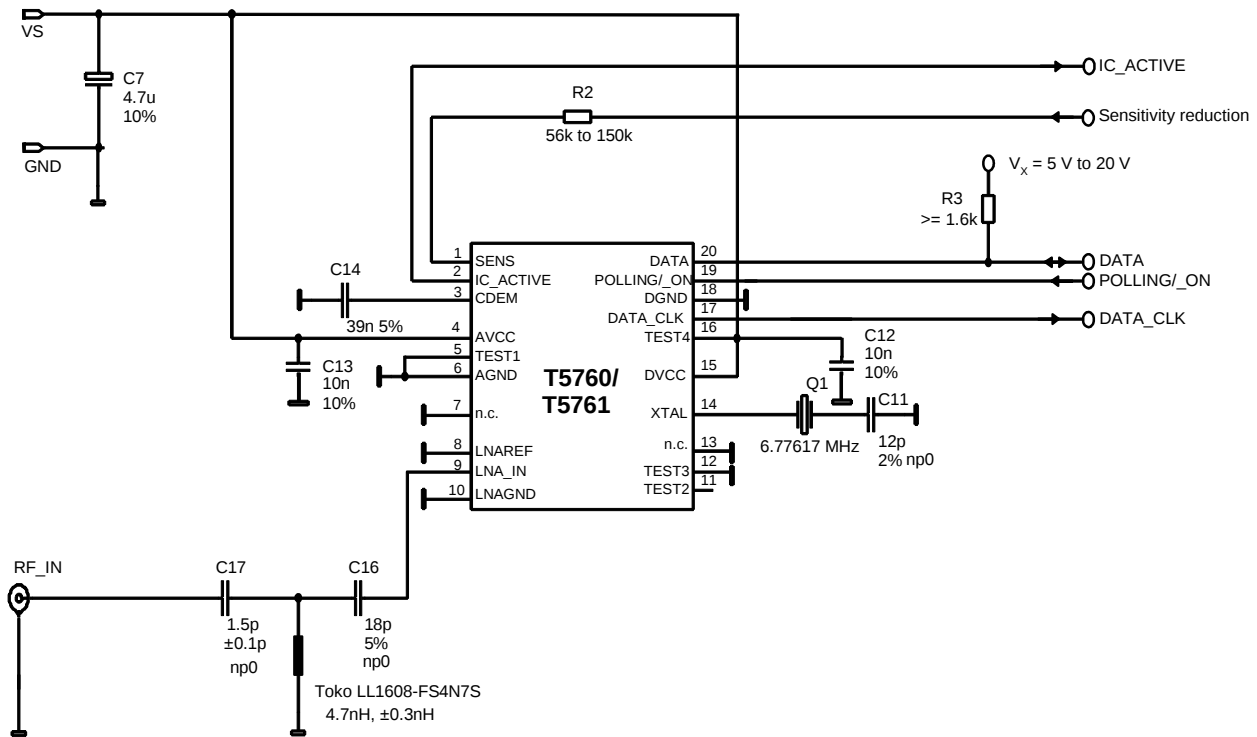
The data interface (see Figure 32) is designed for automotive requirements. It can be connected via the pull-up resistor  $R_{\text{pup}}$  up to 20 V and is short-circuit-protected.

The applicable pull-up resistor  $R_{\text{pup}}$  depends on the load capacity  $C_L$  at Pin DATA and the selected BR\_range (see Table 12).

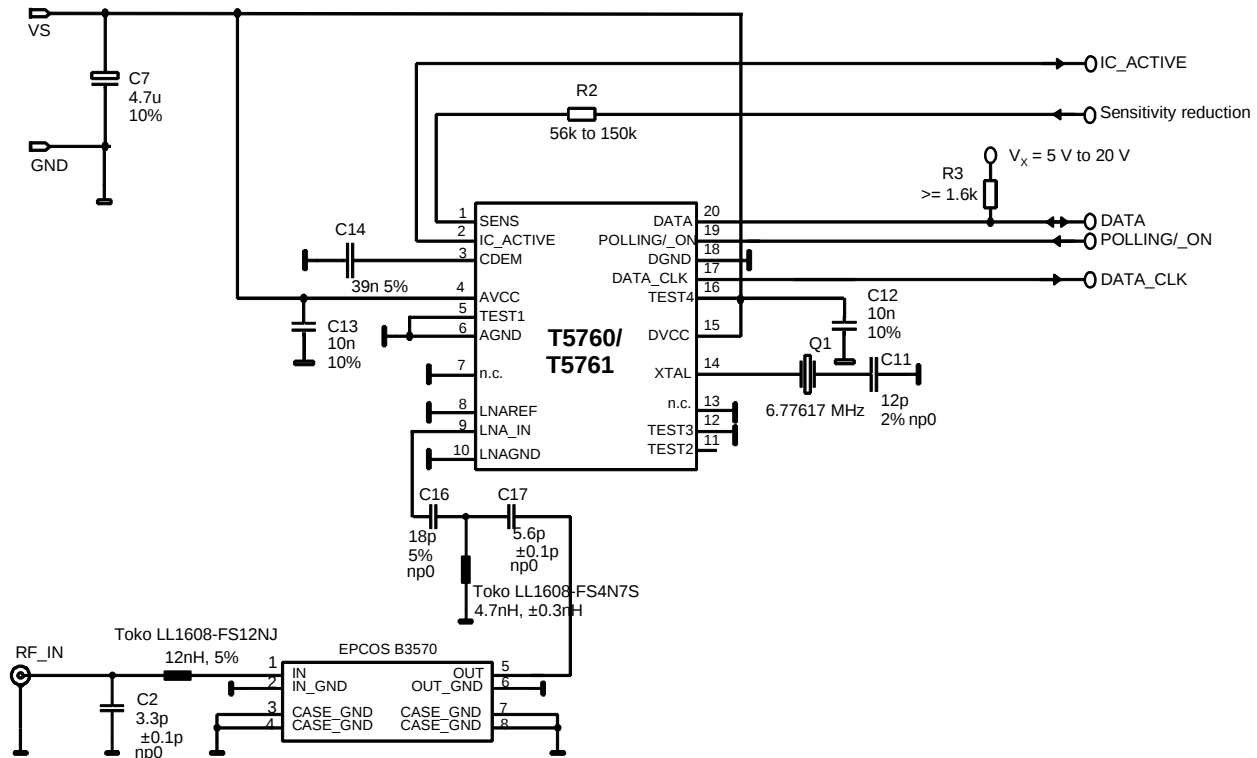
**Table 12.** Applicable  $R_{\text{pup}}$

| -                       | BR_range | Applicable $R_{\text{pup}}$      |
|-------------------------|----------|----------------------------------|
| $C_L \leq 1\text{nF}$   | B0       | 1.6 k $\Omega$ to 47 k $\Omega$  |
|                         | B1       | 1.6 k $\Omega$ to 22 k $\Omega$  |
|                         | B2       | 1.6 k $\Omega$ to 12 k $\Omega$  |
|                         | B3       | 1.6 k $\Omega$ to 5.6 k $\Omega$ |
| $C_L \leq 100\text{pF}$ | B0       | 1.6 k $\Omega$ to 470 k $\Omega$ |
|                         | B1       | 1.6 k $\Omega$ to 220 k $\Omega$ |
|                         | B2       | 1.6 k $\Omega$ to 120 k $\Omega$ |
|                         | B3       | 1.6 k $\Omega$ to 56 k $\Omega$  |

**Figure 33.** Application Circuit:  $f_{RF} = 868.3$  MHz without SAW Filter



**Figure 34.** Application Circuit:  $f_{RF} = 868.3$  MHz with SAW Filter



## Absolute Maximum Ratings

| Parameters                                        | Symbol        | Min. | Max. | Unit |
|---------------------------------------------------|---------------|------|------|------|
| Supply voltage                                    | $V_S$         |      | 6    | V    |
| Power dissipation                                 | $P_{tot}$     |      | 1000 | mW   |
| Junction temperature                              | $T_j$         |      | 150  | °C   |
| Storage temperature                               | $T_{stg}$     | -55  | +125 | °C   |
| Ambient temperature                               | $T_{amb}$     | -40  | +105 | °C   |
| Maximum input level, input matched to 50 $\Omega$ | $P_{in\_max}$ |      | 10   | dBm  |

## Thermal Resistance

| Parameters       | Symbol     | Value | Unit |
|------------------|------------|-------|------|
| Junction ambient | $R_{thJA}$ | 100   | K/W  |

## Electrical Characteristics

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $f_0 = 868.3\text{ MHz}$  and  $f_0 = 915\text{ MHz}$ , unless otherwise specified. (For typical values:  $V_S = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

| Parameter                                           | Test Conditions                                                                                                                       | Symbol                 | f <sub>RF</sub> = 868.3 MHz<br>6.77617 MHz Oscillator |      |                                            | f <sub>RF</sub> = 915 MHz<br>7.14063 MHz Oscillator |      |                                            | Variable Oscillator                                  |      |                                                      | Unit |
|-----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|------------------------|-------------------------------------------------------|------|--------------------------------------------|-----------------------------------------------------|------|--------------------------------------------|------------------------------------------------------|------|------------------------------------------------------|------|
|                                                     |                                                                                                                                       |                        | Min.                                                  | Typ. | Max.                                       | Min.                                                | Typ. | Max.                                       | Min.                                                 | Typ. | Max.                                                 |      |
| Basic Clock Cycle of the Digital Circuitry          |                                                                                                                                       |                        |                                                       |      |                                            |                                                     |      |                                            |                                                      |      |                                                      |      |
| Basic clock cycle                                   |                                                                                                                                       | T <sub>Clk</sub>       | 2.0662                                                |      | 2.0662                                     | 1.9607                                              |      | 1.9607                                     | 14/f <sub>XTO</sub>                                  |      | 14/f <sub>XTO</sub>                                  | μs   |
| Extended basic clock cycle                          | BR_Range0                                                                                                                             | T <sub>XClk</sub>      | 16.53                                                 |      | 16.53                                      | 15.69                                               |      | 15.69                                      | 8 × T <sub>Clk</sub>                                 |      | 8 × T <sub>Clk</sub>                                 | μs   |
|                                                     | BR_Range1                                                                                                                             |                        | 8.26                                                  |      | 8.26                                       | 7.84                                                |      | 7.84                                       | 4 × T <sub>Clk</sub>                                 |      | 4 × T <sub>Clk</sub>                                 | μs   |
|                                                     | BR_Range2                                                                                                                             |                        | 4.13                                                  |      | 4.13                                       | 3.92                                                |      | 3.92                                       | 2 × T <sub>Clk</sub>                                 |      | 2 × T <sub>Clk</sub>                                 | μs   |
|                                                     | BR_Range3                                                                                                                             |                        | 2.07                                                  |      | 2.07                                       | 1.96                                                |      | 1.96                                       | 1 × T <sub>Clk</sub>                                 |      | 1 × T <sub>Clk</sub>                                 | μs   |
| Polling Mode                                        |                                                                                                                                       |                        |                                                       |      |                                            |                                                     |      |                                            |                                                      |      |                                                      |      |
| Sleep time (see Figure 11, Figure 20 and Figure 33) | Sleep and XSleep are defined in the OPMODE register                                                                                   | T <sub>Sleep</sub>     | Sleep × X <sub>Sleep</sub> × 1024 × 2.0662            |      | Sleep × X <sub>Sleep</sub> × 1024 × 2.0662 | Sleep × X <sub>Sleep</sub> × 1024 × 1.9607          |      | Sleep × X <sub>Sleep</sub> × 1024 × 1.9607 | Sleep × X <sub>Sleep</sub> × 1024 × T <sub>Clk</sub> |      | Sleep × X <sub>Sleep</sub> × 1024 × T <sub>Clk</sub> | ms   |
| Start-up time (see Figure 11 and Figure 12)         | BR_Range0                                                                                                                             | T <sub>Startup</sub>   | 1852                                                  |      | 1852                                       | 1758                                                |      | 1758                                       | 896.5                                                |      | 896.5                                                | μs   |
|                                                     | BR_Range1                                                                                                                             |                        | 1059                                                  |      | 1059                                       | 1049                                                |      | 1049                                       | 512.5                                                |      | 512.5                                                | μs   |
|                                                     | BR_Range2                                                                                                                             |                        | 1059                                                  |      | 1059                                       | 1049                                                |      | 1049                                       | 512.5                                                |      | 512.5                                                | μs   |
|                                                     | BR_Range3                                                                                                                             |                        | 662                                                   |      | 662                                        | 628                                                 |      | 628                                        | 320.5 × T <sub>Clk</sub>                             |      | 320.5 × T <sub>Clk</sub>                             | μs   |
| Time for bit check (see Figure 11)                  | Average bit-check time while polling, no RF applied (see Figure 15 and Figure 16)<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | T <sub>Bit-check</sub> |                                                       |      |                                            |                                                     |      |                                            |                                                      |      |                                                      |      |
|                                                     |                                                                                                                                       |                        |                                                       | 0.45 |                                            |                                                     | 0.45 |                                            |                                                      |      |                                                      | ms   |
|                                                     |                                                                                                                                       |                        |                                                       | 0.24 |                                            |                                                     | 0.24 |                                            |                                                      |      |                                                      | ms   |
|                                                     |                                                                                                                                       |                        |                                                       | 0.14 |                                            |                                                     | 0.14 |                                            |                                                      |      |                                                      | ms   |
|                                                     |                                                                                                                                       |                        |                                                       | 0.08 |                                            |                                                     | 0.08 |                                            |                                                      |      |                                                      | ms   |

## Electrical Characteristics (Continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $f_0 = 868.3\text{ MHz}$  and  $f_0 = 915\text{ MHz}$ , unless otherwise specified. (For typical values:  $V_S = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

| Parameter                                                                                                                  | Test Conditions                                                                                                                                               | Symbol             | $f_{RF} = 868.3\text{ MHz}$<br>6.77617 MHz Oscillator |      |                               | $f_{RF} = 915\text{ MHz}$<br>7.14063 MHz Oscillator |      |                               | Variable Oscillator                                                                                                                                      |      |                                                                                                  | Unit                                     |
|----------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------------------------------------------------------|------|-------------------------------|-----------------------------------------------------|------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|------|--------------------------------------------------------------------------------------------------|------------------------------------------|
|                                                                                                                            |                                                                                                                                                               |                    | Min.                                                  | Typ. | Max.                          | Min.                                                | Typ. | Max.                          | Min.                                                                                                                                                     | Typ. | Max.                                                                                             |                                          |
| Time for bit check (see Figure 11)                                                                                         | Bit-check time for a valid input signal $f_{Sig}$ (see Figure 12)<br>$N_{Bit-check} = 0$<br>$N_{Bit-check} = 3$<br>$N_{Bit-check} = 6$<br>$N_{Bit-check} = 9$ | $T_{Bit-check}$    |                                                       |      |                               |                                                     |      |                               | $1 \times T_{XClk}$                                                                                                                                      |      |                                                                                                  | ms                                       |
|                                                                                                                            |                                                                                                                                                               |                    | $3/f_{Sig}$                                           |      | $3.5/f_{Sig}$                 | $3/f_{Sig}$                                         |      | $3.5/f_{Sig}$                 | $3/f_{Sig}$                                                                                                                                              |      | $1 \times T_{Clk}$                                                                               | ms                                       |
|                                                                                                                            |                                                                                                                                                               |                    | $6/f_{Sig}$                                           |      | $6.5/f_{Sig}$                 | $6/f_{Sig}$                                         |      | $6.5/f_{Sig}$                 | $6/f_{Sig}$                                                                                                                                              |      | $6.5/f_{Sig}$                                                                                    | ms                                       |
|                                                                                                                            |                                                                                                                                                               |                    | $9/f_{Sig}$                                           |      | $9.5/f_{Sig}$                 | $9/f_{Sig}$                                         |      | $9.5/f_{Sig}$                 | $9/f_{Sig}$                                                                                                                                              |      | $9.5/f_{Sig}$                                                                                    | ms                                       |
| <b>Receiving Mode</b>                                                                                                      |                                                                                                                                                               |                    |                                                       |      |                               |                                                     |      |                               |                                                                                                                                                          |      |                                                                                                  |                                          |
| Intermediate frequency                                                                                                     |                                                                                                                                                               | $f_{IF}$           |                                                       | 0.95 |                               |                                                     | 1.00 |                               | $f_{RF}/915$                                                                                                                                             |      |                                                                                                  | MHz                                      |
| Baud-rate range                                                                                                            | BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3                                                                                                              | BR_Range           | 1.0<br>1.8<br>3.2<br>5.6                              |      | 1.8<br>3.2<br>5.6<br>10.0     | 1.054<br>1.89<br>3.38<br>5.9                        |      | 1.89<br>3.38<br>5.9<br>10.5   | $BR\_Range0 \times 2 \mu s/T_{Clk}$<br>$BR\_Range1 \times 2 \mu s/T_{Clk}$<br>$BR\_Range2 \times 2 \mu s/T_{Clk}$<br>$BR\_Range3 \times 2 \mu s/T_{Clk}$ |      |                                                                                                  | kBaud<br>kBaud<br>kBaud<br>kBaud         |
| Minimum time period between edges at Pin DATA (see Figure 18 and Figure 19) (With the exception of parameter $T_{Pulse}$ ) | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3                                                                                                | $t_{DATA\_min}$    | 165.3<br>82.6<br>41.3<br>20.7                         |      | 165.3<br>82.6<br>41.3<br>20.7 | 156.8<br>78.4<br>39.2<br>19.6                       |      | 156.8<br>78.4<br>39.2<br>19.6 | $10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$                                                             |      | $10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$     | $\mu s$<br>$\mu s$<br>$\mu s$<br>$\mu s$ |
| Maximum Low period at Pin DATA (see Figure 16)                                                                             | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3                                                                                                | $t_{DATA\_L\_max}$ | 2149<br>1074<br>537<br>269                            |      | 2149<br>1074<br>537<br>269    | 2139<br>1020<br>510<br>255                          |      | 2139<br>1020<br>510<br>255    | $130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$                                                         |      | $130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$ | $\mu s$<br>$\mu s$<br>$\mu s$<br>$\mu s$ |
| Delay to activate the start-up mode (see Figure 22)                                                                        |                                                                                                                                                               | Ton1               | 19.6                                                  |      | 21.7                          | 18.6                                                |      | 20.6                          | $9.5 \times T_{Clk}$                                                                                                                                     |      | $10.5 \times T_{Clk}$                                                                            | $\mu s$                                  |
| OFF command at Pin POLLING/_ON (see Figure 21)                                                                             |                                                                                                                                                               | Ton2               | 16.5                                                  |      |                               | 15.6                                                |      |                               | $8 \times T_{Clk}$                                                                                                                                       |      |                                                                                                  | $\mu s$                                  |
| Delay to activate the sleep mode (see Figure 21)                                                                           |                                                                                                                                                               | Ton3               | 17.6                                                  |      | 19.6                          | 16.6                                                |      | 18.6                          | $8.5 \times T_{Clk}$                                                                                                                                     |      | $9.5 \times T_{Clk}$                                                                             | $\mu s$                                  |
| Pulse on Pin DATA at the end of a data stream (see Figure 30)                                                              | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3                                                                                                | $T_{Pulse}$        | 16.5<br>8.3<br>4.1<br>2.1                             |      | 16.5<br>8.3<br>4.1<br>2.1     | 15.69<br>7.84<br>3.92<br>1.96                       |      | 15.69<br>7.84<br>3.92<br>1.96 | $8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$                                                                     |      | $8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$             | $\mu s$<br>$\mu s$<br>$\mu s$<br>$\mu s$ |

## Electrical Characteristics (Continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $f_0 = 868.3\text{ MHz}$  and  $f_0 = 915\text{ MHz}$ , unless otherwise specified. (For typical values:  $V_S = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

| Parameter                                                   | Test Conditions                                                             | Symbol                  | f <sub>RF</sub> = 868.3 MHz<br>6.77617 MHz Oscillator |      |                                           | f <sub>RF</sub> = 915 MHz<br>7.14063 MHz Oscillator |      |                                  | Variable Oscillator                                                                                                               |      |                                                                                                          | Unit                       |
|-------------------------------------------------------------|-----------------------------------------------------------------------------|-------------------------|-------------------------------------------------------|------|-------------------------------------------|-----------------------------------------------------|------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|------|----------------------------------------------------------------------------------------------------------|----------------------------|
|                                                             |                                                                             |                         | Min.                                                  | Typ. | Max.                                      | Min.                                                | Typ. | Max.                             | Min.                                                                                                                              | Typ. | Max.                                                                                                     |                            |
| Configuration of the Receiver (see Figure 17 and Figure 33) |                                                                             |                         |                                                       |      |                                           |                                                     |      |                                  |                                                                                                                                   |      |                                                                                                          |                            |
| Frequency of the reset marker                               | Frequency is stable within 50 ms after POR                                  | f <sub>RM</sub>         | 118.2                                                 |      | 118.2                                     | 124.5                                               |      | 124.5                            | 1/<br>(4096 × T <sub>Clk</sub> )                                                                                                  |      | 1/<br>(4096 × T <sub>Clk</sub> )                                                                         | Hz                         |
| Programming start pulse                                     | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3<br>after POR | t1                      | 3355<br>2273<br>1731<br>1461<br>16397                 |      | 11637<br>11637<br>11637<br>11637<br>15560 | 3184<br>2168<br>1643<br>1386<br>15560               |      | 11043<br>11043<br>11043<br>11043 | 1624 × T <sub>Clk</sub><br>1100 × T <sub>Clk</sub><br>838 × T <sub>Clk</sub><br>707 × T <sub>Clk</sub><br>7936 × T <sub>Clk</sub> |      | 5632 × T <sub>Clk</sub><br>5632 × T <sub>Clk</sub><br>5632 × T <sub>Clk</sub><br>5632 × T <sub>Clk</sub> | μs<br>μs<br>μs<br>μs<br>μs |
| Programming delay period                                    |                                                                             | t2                      | 795                                                   |      | 797                                       | 754                                                 |      | 756                              | 384.5 × T <sub>Clk</sub>                                                                                                          |      | 385.5 × T <sub>Clk</sub>                                                                                 | μs                         |
| Synchroni-<br>zation pulse                                  |                                                                             | t3                      | 264                                                   |      | 264                                       | 251                                                 |      | 251                              | 128 × T <sub>Clk</sub>                                                                                                            |      | 128 × T <sub>Clk</sub>                                                                                   | μs                         |
| Delay until of the program window starts                    |                                                                             | t4                      | 131                                                   |      | 131                                       | 125                                                 |      | 125                              | 63.5 × T <sub>Clk</sub>                                                                                                           |      | 63.5 × T <sub>Clk</sub>                                                                                  | μs                         |
| Programming window                                          |                                                                             | t5                      | 529                                                   |      | 529                                       | 502                                                 |      | 502                              | 256 × T <sub>Clk</sub>                                                                                                            |      | 256 × T <sub>Clk</sub>                                                                                   | μs                         |
| Time frame of a bit                                         |                                                                             | t6                      | 1058                                                  |      | 1058                                      | 1004                                                |      | 1004                             | 512 × T <sub>Clk</sub>                                                                                                            |      | 512 × T <sub>Clk</sub>                                                                                   | μs                         |
| Programming pulse                                           |                                                                             | t7                      | 132                                                   |      | 529                                       | 125                                                 |      | 502                              | 64 × T <sub>Clk</sub>                                                                                                             |      | 256 × T <sub>Clk</sub>                                                                                   | μs                         |
| Equivalent acknowledge pulse: E_Ack                         |                                                                             | t8                      | 264                                                   |      | 264                                       | 251                                                 |      | 251                              | 128 × T <sub>Clk</sub>                                                                                                            |      | 128 × T <sub>Clk</sub>                                                                                   | μs                         |
| Equivalent time window                                      |                                                                             | t9                      | 533                                                   |      | 533                                       | 506                                                 |      | 506                              | 258 × T <sub>Clk</sub>                                                                                                            |      | 258 × T <sub>Clk</sub>                                                                                   | μs                         |
| OFF-bit programming window                                  |                                                                             | t10                     | 929                                                   |      | 929                                       | 881                                                 |      | 881                              | 449.5 × T <sub>Clk</sub>                                                                                                          |      | 449.5 × T <sub>Clk</sub>                                                                                 | μs                         |
| Data Clock (see Figure 27 and Figure 28)                    |                                                                             |                         |                                                       |      |                                           |                                                     |      |                                  |                                                                                                                                   |      |                                                                                                          |                            |
| Minimum delay time between edge at DATA and DATA_CLK        | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3              | t <sub>Delay2</sub>     | 0<br>0<br>0<br>0                                      |      | 16.5<br>8.3<br>4.1<br>2.1                 | 0<br>0<br>0<br>0                                    |      | 16.7<br>7.8<br>3.9<br>1.96       | 0<br>0<br>0<br>0                                                                                                                  |      | 1 × T <sub>XClk</sub><br>1 × T <sub>XClk</sub><br>1 × T <sub>XClk</sub><br>1 × T <sub>XClk</sub>         | μs<br>μs<br>μs<br>μs       |
| Pulse width of negative pulse at Pin DATA_CLK               | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3              | t <sub>P_DATA_CLK</sub> | 66.1<br>33.0<br>16.5<br>8.3                           |      | 66.1<br>33.0<br>16.5<br>8.3               | 63<br>31<br>15.7<br>7.8                             |      | 63<br>31<br>15.7<br>7.8          | 4 × T <sub>XClk</sub><br>4 × T <sub>XClk</sub><br>4 × T <sub>XClk</sub><br>4 × T <sub>XClk</sub>                                  |      | 4 × T <sub>XClk</sub><br>4 × T <sub>XClk</sub><br>4 × T <sub>XClk</sub><br>4 × T <sub>XClk</sub>         | μs<br>μs<br>μs<br>μs       |

## Electrical Characteristics (continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $f_0 = 868.3\text{ MHz}$  and  $f_0 = 915\text{ MHz}$ , unless otherwise specified. (For typical values:  $V_S = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

| Parameters                                                                                                    | Test Conditions                                                                                                                                                                                        | Symbol            | Min.   | Typ.                                       | Max.       | Unit                                                         |
|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|--------|--------------------------------------------|------------|--------------------------------------------------------------|
| Current consumption                                                                                           | Sleep mode<br>(XTO and polling logic active)                                                                                                                                                           | $I_{S_{off}}$     |        | 170                                        | 276        | $\mu\text{A}$                                                |
|                                                                                                               | IC active (start-up-, bit-check-,<br>receiving mode) Pin DATA = H<br>FSK<br>ASK                                                                                                                        | $I_{S_{on}}$      |        | 7.8<br>7.4                                 | 9.9<br>9.6 | mA<br>mA                                                     |
| <b>LNA, Mixer, Polyphase Lowpass and IF Amplifier (Input Matched According to Figure 33 Referred to RFIN)</b> |                                                                                                                                                                                                        |                   |        |                                            |            |                                                              |
| Third-order intercept point                                                                                   | LNA/mixer/IF amplifier                                                                                                                                                                                 | IIP3              |        | -16                                        |            | dBm                                                          |
| LO spurious emission                                                                                          | Required according to I-ETS 300220                                                                                                                                                                     | $IS_{LORF}$       |        | -70                                        | -57        | dBm                                                          |
| System noise figure                                                                                           | With power matching $ S_{11}  < -10\text{ dB}$                                                                                                                                                         | NF                |        | 5                                          |            | dB                                                           |
| LNA_IN input impedance                                                                                        | at 868.3 MHz<br>at 915 MHz                                                                                                                                                                             | $Z_{i_{LNA\_IN}}$ |        | $200 \parallel 3.2$<br>$200 \parallel 3.2$ |            | $\Omega \parallel \text{pF}$<br>$\Omega \parallel \text{pF}$ |
| 1 dB compression point                                                                                        |                                                                                                                                                                                                        | $IP_{1\text{dB}}$ |        | -25                                        |            | dBm                                                          |
| Image rejection                                                                                               | Within the complete image band                                                                                                                                                                         |                   | 20     | 30                                         |            | dB                                                           |
| Maximum input level                                                                                           | $BER \leq 10^{-3}$ ,<br>FSK mode<br>ASK mode                                                                                                                                                           | $P_{in\_max}$     |        |                                            | -10<br>-10 | dBm<br>dBm                                                   |
| <b>Local Oscillator</b>                                                                                       |                                                                                                                                                                                                        |                   |        |                                            |            |                                                              |
| Operating frequency range VCO                                                                                 | T5760                                                                                                                                                                                                  | $f_{VCO}$         | 866    |                                            | 871        | MHz                                                          |
|                                                                                                               | T5761                                                                                                                                                                                                  | $f_{VCO}$         | 900    |                                            | 929        | MHz                                                          |
| Phase noise local oscillator                                                                                  | $f_{osc} = 867.3\text{ MHz}$ at 10 MHz                                                                                                                                                                 | L (fm)            |        | -140                                       | -130       | dBc/Hz                                                       |
| Spurious of the VCO                                                                                           | at $\pm f_{XTO}$                                                                                                                                                                                       |                   |        | -55                                        | -45        | dBc                                                          |
| XTO pulling                                                                                                   | XTO pulling,<br>appropriate load capacitance must<br>be connected to XTAL,<br>crystal $C_M = 7\text{ fF}$<br>$f_{XTAL} = 6.77617\text{ MHz}$ (EU)<br>$f_{XTAL} = 7.14063\text{ MHz}$ (US)              | $f_{XTO}$         | -30ppm | $f_{XTAL}$                                 | +30ppm     | MHz                                                          |
| Series resonance resistor of the<br>crystal                                                                   | Parameter of the supplied crystal                                                                                                                                                                      | $R_S$             |        |                                            | 120        | $\Omega$                                                     |
| Static capacitance at Pin XTAL to<br>GND                                                                      | Parameter of the supplied crystal<br>and board parasitics                                                                                                                                              | $C_0$             |        |                                            | 6.5        | pF                                                           |
| <b>Analog Signal Processing (Input Matched According to Figure 33 Referred to RFIN)</b>                       |                                                                                                                                                                                                        |                   |        |                                            |            |                                                              |
| Input sensitivity ASK                                                                                         | ASK (level of carrier)<br>$BER \leq 10^{-3}$ , 100% Mod<br>$f_{in} = 868.3\text{ MHz}/915\text{ MHz}$<br>$V_S = 5\text{ V}$ , $T_{amb} = 25^{\circ}\text{C}$<br>$f_{IF} = 950\text{ kHz}/1\text{ MHz}$ | $P_{Ref\_ASK}$    |        |                                            |            |                                                              |
|                                                                                                               | BR_Range0                                                                                                                                                                                              |                   | -110   | -112                                       | -114       | dBm                                                          |
|                                                                                                               | BR_Range1                                                                                                                                                                                              |                   | -108.5 | -110.5                                     | -112.5     | dBm                                                          |
|                                                                                                               | BR_Range2                                                                                                                                                                                              |                   | -108   | -110                                       | -112       | dBm                                                          |
|                                                                                                               | BR_Range3                                                                                                                                                                                              |                   | -106   | -108                                       | -110       | dBm                                                          |

## Electrical Characteristics (continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $f_0 = 868.3\text{ MHz}$  and  $f_0 = 915\text{ MHz}$ , unless otherwise specified. (For typical values:  $V_S = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

| Parameters                                                                                                                                 | Test Conditions                                                                                                                                                                                                                                                                | Symbol                     | Min.            | Typ.                  | Max.             | Unit                 |
|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----------------|-----------------------|------------------|----------------------|
| Sensitivity variation ASK for the full operating range compared to $T_{amb} = 25^{\circ}\text{C}$ , $V_S = 5\text{ V}$                     | $f_{in} = 868.3\text{ MHz}/915\text{ MHz}$<br>$f_{IF} = 950\text{ kHz}/1\text{ MHz}$<br>$P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$                                                                                                                                              | $\Delta P_{Ref}$           | +2.5            |                       | -1.0             | dB                   |
| Sensitivity variation ASK for full operating range including IF filter compared to $T_{amb} = 25^{\circ}\text{C}$ , $V_S = 5\text{ V}$     | $f_{in} = 868.3\text{ MHz}/915\text{ MHz}$<br>$f_{IF} = 950\text{ kHz}/1\text{ MHz}$<br>$f_{IF} -210\text{ kHz to }+210\text{ kHz}$<br>$f_{IF} -270\text{ kHz to }+270\text{ kHz}$<br>$P_{ASK} = P_{Ref\_ASK} + \Delta P_{Ref}$                                                | $\Delta P_{Ref}$           | +5.5<br>+7.5    |                       | -1.5<br>-1.5     | dB<br>dB             |
| Input sensitivity FSK                                                                                                                      | $BER \leq 10^{-3}$<br>$f_{in} = 868.3\text{ MHz}/915\text{ MHz}$<br>$V_S = 5\text{ V}$ , $T_{amb} = 25^{\circ}\text{C}$<br>$f_{IF} = 950\text{ kHz}/1\text{ MHz}$                                                                                                              |                            |                 |                       |                  |                      |
|                                                                                                                                            | BR_Range0<br>$df = \pm 16\text{ kHz to } \pm 28\text{ kHz}$<br>$df = \pm 10\text{ kHz to } \pm 100\text{ kHz}$                                                                                                                                                                 | $P_{Ref\_FSK}$             | -103<br>-101    | -106                  | -107.5<br>-107.5 | dBm<br>dBm           |
|                                                                                                                                            | BR_Range1<br>$df = \pm 16\text{ kHz to } \pm 28\text{ kHz}$<br>$df = \pm 10\text{ kHz to } \pm 100\text{ kHz}$                                                                                                                                                                 | $P_{Ref\_FSK}$             | -101<br>-99     | -104                  | -105.5<br>-105.5 | dBm<br>dBm           |
|                                                                                                                                            | BR_Range2<br>$df = \pm 18\text{ kHz to } \pm 31\text{ kHz}$<br>$df = \pm 13\text{ kHz to } \pm 100\text{ kHz}$                                                                                                                                                                 | $P_{Ref\_FSK}$             | -99.5<br>-97.5  | -102.5                | -104             | dBm<br>dBm           |
|                                                                                                                                            | BR_Range3<br>$df = \pm 25\text{ kHz to } \pm 44\text{ kHz}$<br>$df = \pm 20\text{ kHz to } \pm 100\text{ kHz}$                                                                                                                                                                 | $P_{Ref\_FSK}$             | -97.5<br>-95.5  | -100.5                | -102             | dBm<br>dBm           |
| Sensitivity variation FSK for the full operating range compared to $T_{amb} = 25^{\circ}\text{C}$ , $V_S = 5\text{ V}$                     | $f_{in} = 868.3\text{ MHz}/915\text{ MHz}$<br>$f_{IF} = 950\text{ kHz}/1\text{ MHz}$<br>$P_{FSK} = P_{Ref\_FSK} + \Delta P_{Ref}$                                                                                                                                              | $\Delta P_{Ref}$           | +3              |                       | -1.5             | dB                   |
| Sensitivity variation FSK for the full operating range including IF filter compared to $T_{amb} = 25^{\circ}\text{C}$ , $V_S = 5\text{ V}$ | $f_{in} = 868.3\text{ MHz}/915\text{ MHz}$<br>$f_{IF} = 950\text{ kHz}/1\text{ MHz}$<br>$f_{IF} -150\text{ kHz to }+150\text{ kHz}$<br>$f_{IF} -200\text{ kHz to }+200\text{ kHz}$<br>$f_{IF} -260\text{ kHz to }+260\text{ kHz}$<br>$P_{FSK} = P_{Ref\_FSK} + \Delta P_{Ref}$ | $\Delta P_{Ref}$           | +6<br>+8<br>+11 |                       | -2<br>-2<br>-2   | dB<br>dB<br>dB       |
| S/N ratio to suppress inband noise signals. Noise signals may have any modulation scheme                                                   | ASK mode<br>FSK mode                                                                                                                                                                                                                                                           | $SNR_{ASK}$<br>$SNR_{FSK}$ |                 | 10<br>2               | 12<br>3          | dB<br>dB             |
| Dynamic range RSSI amplifier                                                                                                               |                                                                                                                                                                                                                                                                                | $DR_{RSSI}$                |                 | 60                    |                  | dB                   |
| Lower cut-off frequency of the data filter                                                                                                 | $f_{cu\_DF} = \frac{1}{2 \times \pi \times 30\text{ k}\Omega \times CDEM}$<br>$CDEM = 33\text{ nF}$                                                                                                                                                                            | $f_{cu\_DF}$               | 0.11            | 0.16                  | 0.20             | kHz                  |
| Recommended CDEM for best performance                                                                                                      | BR_Range0 (default)<br>BR_Range1<br>BR_Range2<br>BR_Range3                                                                                                                                                                                                                     | CDEM                       |                 | 39<br>22<br>12<br>8.2 |                  | nF<br>nF<br>nF<br>nF |

## Electrical Characteristics (continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $f_0 = 868.3\text{ MHz}$  and  $f_0 = 915\text{ MHz}$ , unless otherwise specified. (For typical values:  $V_S = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

| Parameters                                                                                                                                                                                                                                    | Test Conditions                                                                                                                                                                                                                                                                                                      | Symbol                                                                                                      | Min.                                            | Typ.                                        | Max.                                                        | Unit                                                                   |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|-------------------------------------------------|---------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------------------|
| Edge-to-edge time period of the input data signal for full sensitivity                                                                                                                                                                        | BR_Range0 (default)<br>BR_Range1<br>BR_Range2<br>BR_Range3                                                                                                                                                                                                                                                           | $t_{ee\_sig}$                                                                                               | 270<br>156<br>89<br>50                          |                                             | 1000<br>560<br>320<br>180                                   | ms<br>ms<br>ms<br>ms                                                   |
| Upper cut-off frequency data filter                                                                                                                                                                                                           | Upper cut-off frequency programmable in 4 ranges via a serial mode word<br>BR_Range0 (default)<br>BR_Range1<br>BR_Range2<br>BR_Range3                                                                                                                                                                                | $f_u$                                                                                                       | 2.8<br>4.8<br>8.0<br>15.0                       | 3.4<br>6.0<br>10.0<br>19.0                  | 4.0<br>7.2<br>12.0<br>23.0                                  | kHz<br>kHz<br>kHz<br>kHz                                               |
| Reduced sensitivity                                                                                                                                                                                                                           | $R_{Sense}$ connected from Pin Sens to $V_S$ , input matched according to Figure 33,<br>$f_{IN} = 868.3\text{ MHz}/915\text{ MHz}$ , $V_S = 5\text{ V}$ ,<br>$T_{amb} = +25^{\circ}\text{C}$                                                                                                                         |                                                                                                             |                                                 |                                             |                                                             | dBm (peak level)                                                       |
|                                                                                                                                                                                                                                               | $R_{Sense} = 56\text{ k}\Omega$                                                                                                                                                                                                                                                                                      | $P_{Ref\_Red}$                                                                                              | -63                                             | -68                                         | -73                                                         | dBm                                                                    |
|                                                                                                                                                                                                                                               | $R_{Sense} = 100\text{ k}\Omega$                                                                                                                                                                                                                                                                                     | $P_{Ref\_Red}$                                                                                              | -72                                             | -77                                         | -82                                                         | dBm                                                                    |
| Reduced sensitivity variation over full operating range                                                                                                                                                                                       | $R_{Sense} = 56\text{ k}\Omega$<br>$R_{Sense} = 100\text{ k}\Omega$<br>$P_{Red} = P_{Ref\_Red} + \Delta P_{Red}$                                                                                                                                                                                                     | $\Delta P_{Red}$                                                                                            | 5<br>5                                          | 0<br>0                                      | 0<br>0                                                      | dB<br>dB                                                               |
| Reduced sensitivity variation for different values of $R_{Sense}$                                                                                                                                                                             | Values relative to $R_{Sense} = 56\text{ k}\Omega$<br>$R_{Sense} = 56\text{ k}\Omega$<br>$R_{Sense} = 68\text{ k}\Omega$<br>$R_{Sense} = 82\text{ k}\Omega$<br>$R_{Sense} = 100\text{ k}\Omega$<br>$R_{Sense} = 120\text{ k}\Omega$<br>$R_{Sense} = 150\text{ k}\Omega$<br>$P_{Red} = P_{Ref\_Red} + \Delta P_{Red}$ | $\Delta P_{Red}$                                                                                            |                                                 | 0<br>-3.5<br>-6.0<br>-9.0<br>-11.0<br>-13.5 |                                                             | dB<br>dB<br>dB<br>dB<br>dB<br>dB                                       |
| Threshold voltage for reset                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                      | $V_{ThRESET}$                                                                                               | 1.95                                            | 2.8                                         | 3.75                                                        | V                                                                      |
| <b>Digital Ports</b>                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                      |                                                                                                             |                                                 |                                             |                                                             |                                                                        |
| Data output<br>- Saturation voltage Low<br><br>- max voltage at Pin DATA<br>- quiescent current<br>- short-circuit current<br>- ambient temp. in case of permanent short-circuit<br>Data input<br>- Input voltage Low<br>- Input voltage High | $I_{ol} \leq 12\text{ mA}$<br>$I_{ol} = 2\text{ mA}$<br><br>$V_{oh} = 20\text{ V}$<br>$V_{ol} = 0.8\text{ V}$ to $20\text{ V}$<br>$V_{oh} = 0\text{ V}$ to $20\text{ V}$                                                                                                                                             | $V_{ol}$<br>$V_{ol}$<br>$V_{oh}$<br>$I_{qu}$<br>$I_{ol\_lim}$<br>$t_{amb\_sc}$<br><br>$V_{ll}$<br>$V_{ich}$ | <br><br><br>13<br><br><br><br>0.65 $\times V_S$ | 0.35<br>0.08<br><br>30                      | 0.8<br>0.3<br>20<br>20<br>45<br>85<br><br>$0.35 \times V_S$ | V<br>V<br>V<br>$\mu\text{A}$<br>mA<br>$^{\circ}\text{C}$<br><br>V<br>V |
| DATA_CLK output<br>- Saturation voltage Low<br>- Saturation voltage High                                                                                                                                                                      | IDATA_CLK = 1mA<br>IDATA_CLK = -1mA                                                                                                                                                                                                                                                                                  | $V_{ol}$<br>$V_{oh}$                                                                                        | <br>$V_S - 0.4\text{ V}$                        | 0.1<br>$V_S - 0.15\text{ V}$                | 0.4                                                         | V<br>V                                                                 |
| IC_ACTIVE output<br>- Saturation voltage Low<br>- Saturation voltage High                                                                                                                                                                     | IIC_ACTIVE = 1 mA<br>IIC_ACTIVE = -1 mA                                                                                                                                                                                                                                                                              | $V_{ol}$<br>$V_{oh}$                                                                                        | <br>$V_S - 0.4\text{ V}$                        | 0.1<br>$V_S - 0.15\text{ V}$                | 0.4                                                         | V<br>V                                                                 |

## Electrical Characteristics (continued)

All parameters refer to GND,  $T_{amb} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_S = 4.5\text{ V}$  to  $5.5\text{ V}$ ,  $f_0 = 868.3\text{ MHz}$  and  $f_0 = 915\text{ MHz}$ , unless otherwise specified. (For typical values:  $V_S = 5\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ )

| Parameters                                                                   | Test Conditions                       | Symbol               | Min.             | Typ. | Max.             | Unit   |
|------------------------------------------------------------------------------|---------------------------------------|----------------------|------------------|------|------------------|--------|
| POLLING/_ON input<br>- Low level input voltage<br>- High level input voltage | Receiving mode<br>Polling mode        | $V_{ll}$<br>$V_{lh}$ | $0.8 \times V_S$ |      | $0.2 \times V_S$ | V<br>V |
| TEST 4 pin<br>- High level input voltage                                     | Test input must always be set to High | $V_{lh}$             | $0.8 \times V_S$ |      |                  | V      |
| TEST 1 pin<br>- Low level input voltage                                      | Test input must always be set to Low  | $V_{ll}$             |                  |      | $0.2 \times V_S$ | V      |

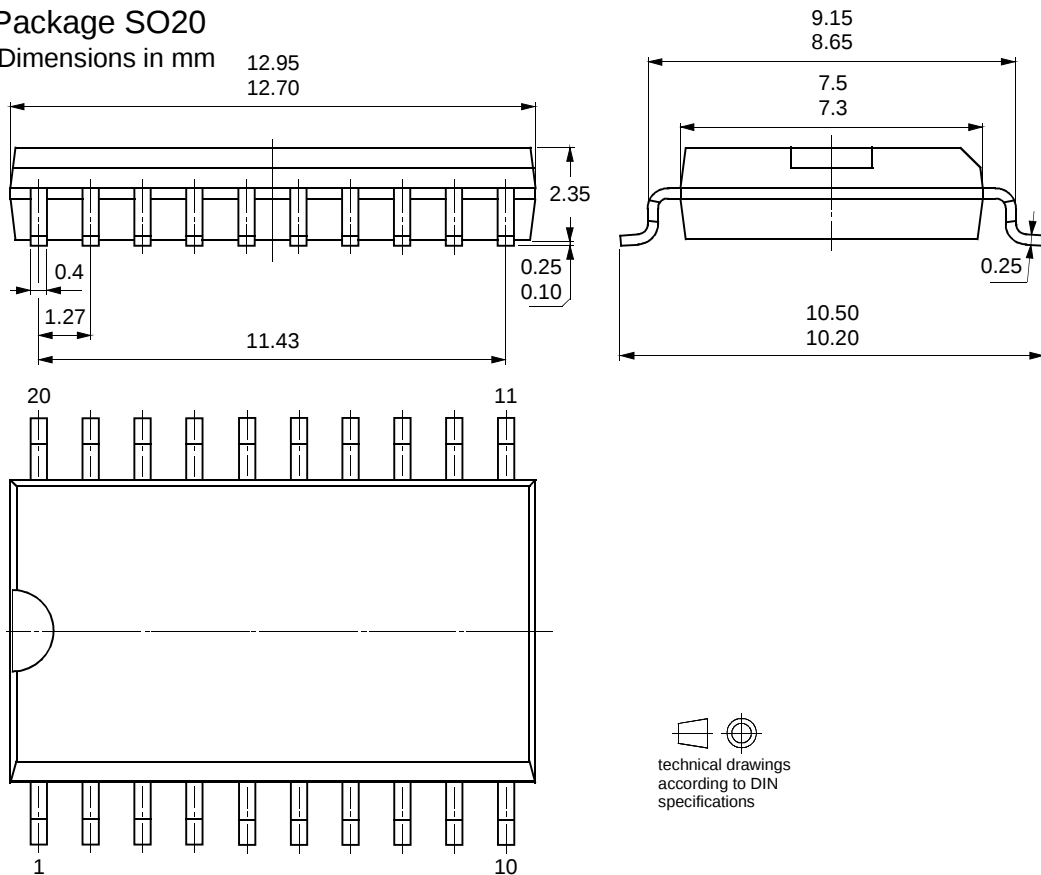
## Ordering Information

| Extended Type Number | Package | Remarks                                |
|----------------------|---------|----------------------------------------|
| T5760-TGS            | SO20    | Tube, for 868 MHz ISM band             |
| T5760-TGQ            | SO20    | Taped and reeled, for 868 MHz ISM band |
| T5761-TGS            | SO20    | Tube, for 915 MHz ISM band             |
| T5761-TGQ            | SO20    | Taped and reeled, for 915 MHz ISM band |

## Package Information

### Package SO20

Dimensions in mm





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